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Smart Bias Controller Design for HEMT amplifier for use in jamming applications.

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HEMT amplifier Bias controller design for jamming applications.

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Abstract

This thesis presents the simulation and creation of a bias controller for a GaN RF amplifier. GaN RF amplifiers are known for their high efficiency and versatility, making them suitable for a variety of applications, including jamming. However, a key challenge with these devices is that they can burn out if not powered correctly. The bias controller presented in this thesis addresses this issue by providing a precise sequence of power to the gate and drain of the GaN amplifier.

The bias controller was designed and simulated to ensure that the GaN amplifier operates within its safe operating conditions. The results of the simulation were validated through the creation of a physical PCB, which was tested and verified to function as expected. The implementation of the bias controller led to increased reliability and efficiency for the GaN RF amplifier.

The key contribution of this thesis is the development of a new and effective solution for powering GaN RF amplifiers. The simulation and physical implementation demonstrate the viability of the bias controller and its potential impact on future development and applications in electronics and RF amplification. The research in this thesis highlights the importance of proper power sequencing for GaN RF amplifiers and provides a new and innovative approach for ensuring their reliability and performance.

Thanks

First of all, I would like to thank my family for their support provided during my studies in the Masters Program in Computer Security

I would also like to thank Supervising Professor Dr. Iliana Stavrou, who gave me the directions for the right approach to the subject and the conducting the research. I express my gratitude, both for the advice and for her guidance in the implementation of the experimental part of this Thesis.

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Intro

Thesis Structure.

This thesis is structured into chapters, each focusing on key aspects of jamming applications and GaN amplifier technology in the context of cybersecurity.

The first chapter, Jamming in Cybersecurity: This chapter delves into the history, techniques, and applications of jamming in cybersecurity, covering both its military origins and modern uses.

The second chapter, GaN Amplifiers: Here, the focus shifts to the technical aspects of GaN (Gallium Nitride) technology. It explores the reasons GaN outperforms traditional amplifiers, discusses the challenges in its application, and provides a detailed history of its development.

The Third chapter, covers the existing bibliography on the subject. An in-depth review of the current literature and research in the fields of jamming and GaN amplifiers, providing a foundation for the subsequent methodology and implementation chapters

The Forth chapter describes the methodology; the approach and steps taken in the research, including system description, implementation steps, and simulations that underpin the thesis.

The Fifth Chapter covers the implementation: A detailed account of the practical application, covering design requirements, component selection, simulation assumptions, and the systematic implementation of the GaN amplifier, including its various subsystems and components.

The Sixth and final chapter covers the pcb design and the specifics of designing the printed circuit board (PCB) for the GaN amplifier, encapsulating theoretical and practical work detailed in previous chapters.

Each chapter is designed to provide a thorough understanding of the subject, blending historical perspectives with current technological insights and future implications. The structure is crafted to guide the reader through the complexities of both jamming in cybersecurity and the advancements in GaN technology, highlighting their significance in modern communication and defence systems.

1 Jamming in Cyber security.

1.1 Introduction

Since the use of wireless communication technology entered the military environment, the interception of such communications and the use thereof resulting information provides valuable advantages. The devices for jamming in communications was developed and first-used by the military.

Jamming is an act of interference by which the communication signals are blocked or reduced. In jamming, an unwanted signal is transmitted at the same frequency as the intended signal. Both the intended and the unwanted signals are received at the receiving end, but the wanted signal is not received properly because of the unwanted signal. In jamming, the unwanted signal is stronger than the wanted signal, so the wanted signal is not received properly. Jamming is also known as “Interference”, “Blocking”, “Interference Blocking”, “Broadcasting Interference” and “Broadcast Jamming”.

The history of jamming wireless communications can be traced back to the early 20th century, when radio signals were first used for communication. During World War I, both sides in the conflict used jamming to disrupt enemy radio communications. It is likely that jamming was also used during other conflicts in the early 20th century, although there is less information available about these cases. The use of jamming became more widespread and sophisticated during World War II, when both the Allies and the Axis powers used jamming techniques to disrupt enemy radio communications. In the 1950s and 1960s, jamming became more sophisticated and was used by the military to block enemy radar and radio signals.

In the modern era, jamming is still used by military forces to disrupt enemy communications, but it is also used by governments and organizations to block or interfere with certain types of communication in order to prevent the spread of information or to protect national security (for example it would be its used in an air gapped or high security government buildings where all wireless communications must be blocked). In addition, jamming is sometimes used by individuals or groups to disrupt communication for criminal or malicious purposes.

Now days Jamming is often employed during cyber-attacks and cyber warfare. The signals that jamming interferes with are those that are transmitted in the air, such as Wi-Fi, Bluetooth, and radio frequencies.

A common example of jamming is when a radio station is broadcasted on the same frequency as that of a nearby radio station with weaker signal strength and thereby drowning the weaker signal out.

Jamming is used in cyber security to disrupt the communication signals of the cyber attackers. Jamming can be used to prevent cyber attackers from accessing the network or to prevent them from accessing critical information

1.2 Wireless signals and RF.

All the wireless signals that are used in the modern world for communications they are using RF (radio frequencies).

Radio frequency (RF) [1], is a measurement representing the oscillation rate of electromagnetic radiation spectrum, or electromagnetic radio waves, from frequencies ranging from 300 gigahertz (GHz) to as low as 9 kilohertz (kHz). With the use of antennas and transmitters, an RF field can be used for various types of wireless broadcasting and communications.

Radio frequency is measured in units called hertz (Hz), which represent the number of cycles per second when a radio wave is transmitted. One hertz equals one cycle per second; radio waves range from thousands (kilohertz) to millions (megahertz) to billions (gigahertz) of cycles per second. In a radio wave, the wavelength is inversely proportional to the frequency. Radio frequencies are not visible to the human eye. As the frequency is increased beyond that of the RF spectrum, electromagnetic energy takes the form of microwaves, infrared radiation (IR), visible, ultraviolet, X-rays and gamma rays

Radio Frequencies are divided in licensed and unlicensed bands [2]. Depending on the country, there are government commissions that issue licences that permit commercial entities to have exclusive use of a frequency band in a given location.

Entities include frequency modulation (FM) radio, cellular networks, television, military and satellite communications. Unlicensed frequencies are free for public use but remain a shared medium. [3]

The competition for bandwidth and channels from internet users has increased dramatically in recent years, leading to signal issues. In addition, distribution across frequencies is not equitable. In many locations, it is possible to find broadcasters -- radio and TV stations -- with their own individual frequencies, while a multitude of sources compete for space on the unlicensed frequencies.

1.3 Wireless network vulnerabilities

Due to the nature of electromagnetic propagation, when a wireless signal is transmitted, is not directed exclusively at the receiver but it is transmitted openly in all directions and limited only from the laws of physics and the interaction of the signal and its environment. This ensures that a wireless transmission can never be considered private and confidential.

There are three attack mechanisms that can be used on wireless system: Interference, Spoofing and Jamming. [4]

Interference is intended to extract the information being transmitted from the wireless system. It is difficult to detect an attack like this on a wireless network because passive techniques can be used to demodulate and decode the signal without affecting the integrity of the signal.

Spoofing usually involves injecting packets into wireless systems causing either small effects, such as for example an increase of the bit error rate (BER) or even mass errors in the data. One of the most obvious examples of spoofing is the alteration of Global Positioning System (GPS) location data

jamming is the process of introducing noise into an RF channel in order to block its availability. Jamming on its own has various types:

- Broadcast Jamming: Broadcast jamming is the intentional broadcast of a radio frequency signal in the same frequency as the original signal.
- Directional Jamming: In directional jamming, the unwanted signal is directed towards the receiver of the signal.
- Spreading Jamming: In spreading jamming, the jamming signal is sent over a large area so that the jamming signal interferes with all the communication signals in the area.
- Feedback Jamming: Feedback jamming is the transmission of a signal from the receiver to the transmitter that interferes with the broadcasting signal.
- Selective Jamming: In selective jamming, the jamming signal is targeted toward certain receivers of the signal.

As mentioned before most of the most popular technologies nowadays use bands of RF spectrum, including but not limited to:

- Wifi 2.4G
- Wifi 5G
- LTE and 4g
- Gsm,
- Gps.

So for a successful jamming applications, a very wide band interference signal must be broadcasted, starting from around 700mhz, and reaching up to 6Ghz, while at the same time some critical frequencies and bands in-between must remain unblocked / unjammed.

1.4 Broad casting RF.

Dealing with RF signals in their physical circuits is always a challenge. The high-frequency signals, which are at low voltage levels, need to be boosted to higher power levels to be broadcast. Using a RF amplifier boosts and modifies the signals.

RF Amplifiers have a wide range of applications. Whenever people need to magnify a radio frequency signal into a higher power signal, the RF amplifier plays a pivotal role. The main characteristics of an RF amplifier are linearity, efficiency, output power, and signal gain. They are used in commercial and defence avionics, space and deep space, electronic warfare, naval applications, mobile internet, satellite communication, and wireless communications. [5]

Because of all that, for an effective broadcast of a jamming signal an RF amplifier is needed to boost the signal to the needed level. More specifically a type of RF amplifier that is called Broadband Amplifier, and which has a flat response over a range of frequencies. [6] The state-of-the-art technology for broadband RF amplifiers are GaN HEMP Amplifiers, which would be the type of the amplifier that will be used for this thesis.

1.4.1 International Perspective on jamming.

The use of jamming technology is a matter of significant interest in international relations, as it intersects with issues of sovereignty, defense, and international law. Different countries have varied stances on the use of jamming, often reflecting their broader military and political strategies. For instance, nations with a strong emphasis on information control, such as North Korea or China, have been known to employ jamming techniques to suppress external information sources that could challenge the state narrative

At the international level, there are several treaties and conventions that indirectly influence the use of jamming technology. For example, the International Telecommunication Union (ITU) sets global standards for electromagnetic spectrum usage, which can impact how jamming is regulated. The Geneva Conventions and various UN resolutions also indirectly address the use of jamming, especially in the context of warfare, where jamming can be seen as a tool that interferes with communication in conflict zones. In some cases, jamming is protested as a violation of

free speech or an act of aggression, especially when it interferes with civilian communication channels. In other cases, it's seen as a legitimate tool for national security. This presents a complex landscape where the legality and acceptance of jamming are often contingent on the specific circumstances and the geopolitical context.

1.4.2 Legal And Ethical Considerations.

The legality of jamming depends heavily on national laws, which can vary significantly from country to country. In many jurisdictions, the use of jamming equipment is heavily regulated or outright banned, especially in civilian contexts. For example, in the United States, the Federal Communications Commission [7] (FCC) prohibits the use of jamming devices by civilians, with strict penalties for violations. However, exemptions exist for federal agencies under certain conditions. [8]

Similarly, Jammers [9] are often used around jails and detention centres to prevent inmates and detainees from unauthorized and unmonitored communication with the outside world. Brazil, India, New Zealand and Sweden are countries that have exempted or are considering exemptions for the use of cell phone and Wifi jammers around jails, while in the UK this has been legal since 2012. There are, however, countries that have allowed or have proposed expanding the use of jammers. In India, for example, there are provisions for using jammers in schools, mosques and theatres, provided it can be shown that the interference does not extend beyond their walls. For a brief period, jammers were approved for use also in places like theatres and concert venues, but that ended in 2012.

Whatever the case, the usage of jamming technologies is illegal for individuals, and many countries in the European Union (including Switzerland) with amendments to the Telecommunications Act (TCA), have strictly prohibited the import and possession of gsm jammer.

For this reason, it is recommended that this thesis doesn't go into public domain. Even though the circuit to generate the noise source is not included in this thesis, the amplifier is an important piece of the puzzle.

2 Gan Amplifiers

2.1 What is GaN technology, and why it outperforms other types of amplifiers.

A GaN RF amplifier is a type of amplifier that uses gallium nitride (GaN) as the active material in the amplifier's transistor. GaN is a wide bandgap semiconductor material that is known for its high electron mobility and high breakdown voltage, which makes it ideal for use in high-power, high-frequency applications. [10]

GaN RF amplifiers are commonly used in wireless communication systems, such as cellular phones and radio transmitters, because they can provide high power output and efficient amplification at frequencies up to 6 GHz or higher. They are also used in radar systems and other high-frequency applications.

One of the main reasons that GaN RF amplifiers outperform traditional amplifiers is their ability to operate at higher frequencies and higher power levels. Traditional amplifier technologies, such as silicon or gallium arsenide, tend to become less efficient and have a lower power output as the frequency increases. GaN, on the other hand, can maintain high efficiency and power output at higher frequencies, making it an ideal choice for high-frequency applications.

In addition to their high power and efficiency, GaN RF amplifiers have a number of other benefits over traditional amplifiers. [11] They have a smaller physical size, making them easier to integrate into compact systems. They also have a faster switching speed, which allows them to respond more quickly to changes in input signal. Overall, GaN RF amplifiers offer improved performance and versatility compared to traditional amplifier technologies, making them an attractive choice for a wide range of high-frequency applications.

Some additional reasons why GaN amplifiers stand out for RF applications [12] are:

1. High breakdown field: Because of GaN's large bandgap, the GaN material has a high breakdown field, which allows the GaN device to operate at much higher voltages than other semiconductor devices. When subjected to high enough electric fields, the electrons in the semiconductor can acquire enough kinetic energy to break the chemical bond. If that process is not controlled, it can degrade the device. Because GaN devices can operate at higher voltages, they can be used in higher-power applications.

2. High saturation velocity: Electrons on GaN have a high saturation velocity (the velocity of electrons at very high electric fields). When combined with the large charge capability, this means that GaN devices can deliver much higher current density.

The RF power output is the product of the voltage and the current swings, so a higher voltage and current density can produce higher RF power in a practically sized transistor. Simply put, GaN devices can produce much higher power density.

3. Outstanding thermal properties: GaN devices exhibit outstanding thermal properties, due largely to the high thermal conductivity of SiC. In practical terms, this means that GaN devices don't get as hot as GaAs or Si devices when dissipating the same power, and a "colder" device means a more reliable device

Amplifier Technologies Comparison	GaN on SiC	GaAs (galium arsenide)	Ldmos
Operating Voltage	High	Low	High
Power Density	High	Low	Low
Thermal Resistance	Low	Medium	Medium
Bandwidth	Wide	Wide	Narrow

2.2 Problems using GaN Technology.

There are several challenges that can arise when using GaN RF amplifiers:

High cost: GaN RF amplifiers tend to be more expensive than traditional amplifier technologies, such as silicon or gallium arsenide. This can be a significant barrier for some applications that require large quantities of amplifiers or have strict cost constraints. However this is usually mitigated by the fact that you need multiple amplifiers to get similar wideband or performance.

Thermal management: While GaN RF amplifiers are cooler in general (as mentioned previously in this document) they can generate a significant amount of heat during operation, which can be a challenge to manage. Proper thermal management is crucial to ensure that the amplifier operates within its temperature limits and maintains its performance over time, so any circuit that controls and drive the amplifier must be aware of its temperature all the time and act accordingly.

Driver complexity: The most significant problem is that GaN transistors are depletion mode devices and so require a negative voltage for the gate and a positive voltage for the drain. Moreover, since they are depletion mode devices it is critically important to supply a negative voltage to the gate before any positive voltage is applied to the drain, otherwise the transistor will draw its maximum possible drain current from the supply which is for all terms and purposes and short circuit. This will lead to excessive

thermal dissipation and the device burning out. This phenomenon as well as other details that will explained later call for a smart dynamic biasing circuit.

2.3 Gan Information.

2.3.1 What is a GaN and the basics of MOSFETs

A GaN is a type of MOSFET (metal-oxide-semiconductor field-effect transistor). A MOSFET is a type of transistor that uses a voltage applied to a pin called Gate, to control the flow of current through the device.

MOSFETs are widely used in a variety of electronic circuits and devices, including amplifiers, switches, and voltage regulators. Because they have a high input impedance and can switch quickly, making them useful for high-frequency applications. They are also relatively simple to fabricate and can be made with a small physical footprint, making them suitable for use in portable and compact electronic devices.

A (MOSFET) has three main terminals, or pins, which are typically labeled as the source, drain, and gate. The source and drain are the two main terminals through which current flows in the device, and the gate is used to control the flow of current between the source and drain.

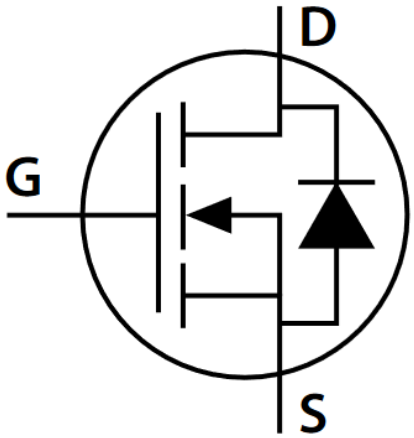

Figure 1. Typical MOSFET Symbol in schematics

The source and drain are typically labeled as such because they are the terminals through which current enters and exits the device, respectively. The gate is named as

such because it controls the flow of current through the device by forming an electric field that modulates the conductivity of the channel between the source and drain.

In addition to the source, drain, and gate, MOSFETs may also have a fourth terminal, called the body or substrate, which is typically connected to the source terminal. The body terminal is used to control the threshold voltage of the device, which determines the range of gate voltages over which the device can be fully turned off or on.[1]

It is important to note that the names and functions of the terminals of a MOSFET may vary depending on the specific type of device and the circuit in which it is being used.

There are 2 categories of MOSFETs and 2 types on each category. [13] The 2 Categories are the N-channel and the P-channel, and they differ in the type of charge carrier used in the channel region between the source and drain terminals.

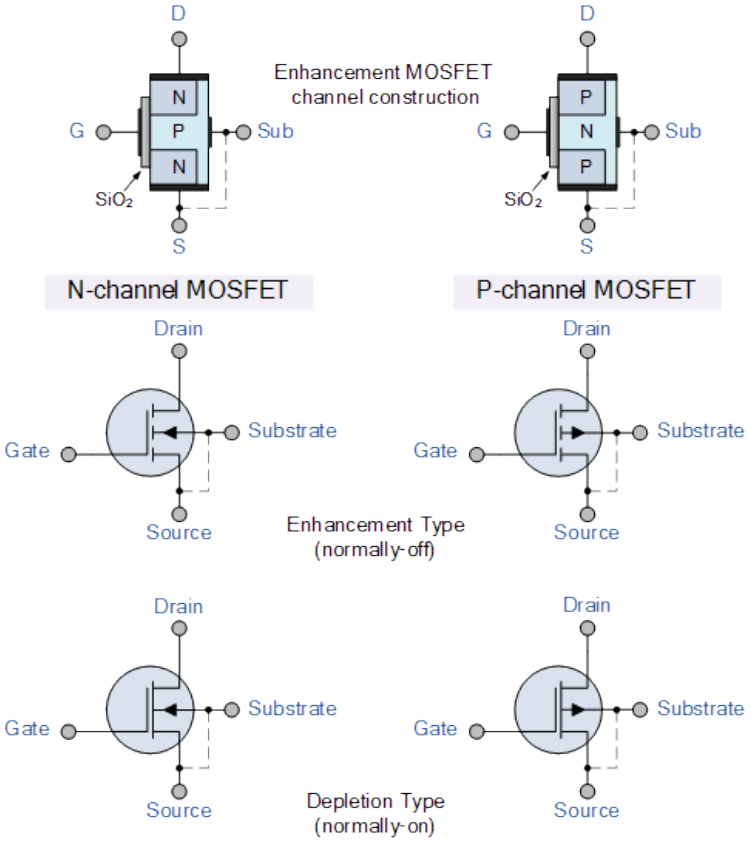

Figure 2. Symbols for all types of MOSFETs

[1] https://www.electronicshub.org/MOSFET/

An n-channel MOSFET uses electrons, which are negatively charged particles, as the charge carriers in the channel. A voltage applied to the gate terminal of an n-channel MOSFET creates an electric field that attracts electrons from the channel, reducing the conductivity of the channel and turning off the device.

A p-channel MOSFET, on the other hand, uses holes, which are the absence of electrons and can be thought of as positively charged particles, as the charge carriers in the channel. A voltage applied to the gate terminal of a p-channel MOSFET creates an electric field that repels holes from the channel, increasing the conductivity of the channel and turning on the device.

N-channel and P-channel MOSFETs have different characteristics and are used in different types of circuits. N-channel MOSFETs are typically faster and more efficient than P-channel MOSFETs, but have a lower voltage rating and are more sensitive to temperature. P-channel MOSFETs have a higher voltage rating and are less sensitive to temperature, but are slower and less efficient than N-channel MOSFETs.

In simpler terms a N-Channel MOSFET is used as a ‘Low-side” switch, ie, a switch that is inserted into the negative/ground return of the circuit being powered.

Similarly, a P-channel MOSFET is used as a ‘High-Side” switch, ie a switch that is inserted in series with the positive/supply to the circuit being powered.

The difference between the tew is illustrated with these two simple examples:

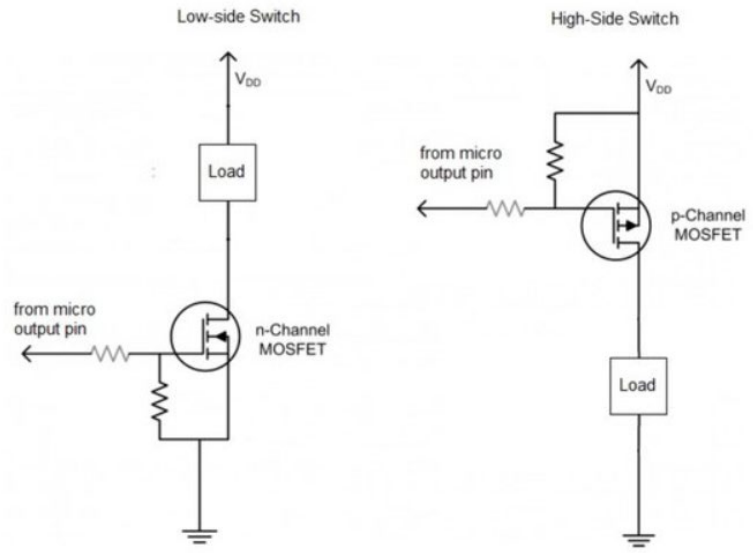

Figure 3. N-Channel and P-Channel Usage

There are also two main types of MOSFETs: enhancement mode and depletion mode. Enhancement mode MOSFETs require a positive voltage applied to the gate to turn on the device and allow current to flow through it. Depletion mode MOSFETs, on the other hand, are normally on and require a negative voltage (pinch-off voltage) applied to the gate to turn off the device and stop current flow.

The pinch-off voltage of a depletion mode device, also known as the threshold voltage, is the voltage at which the device begins to turn off or stop conducting current. In a depletion mode transistor, such as a depletion mode MOSFET, the pinch-off voltage is the voltage at which the channel between the source and drain becomes depleted of charge carriers and the device stops conducting.

The pinch-off voltage is an important parameter in the operation of depletion mode devices, as it determines the range of gate voltages over which the device can be fully turned off or on. The pinch-off voltage can be adjusted by adjusting the gate-to-source voltage of the device, allowing for precise control of the device's conductivity.

It is important to note that the pinch-off voltage is different from the turn-on voltage of an enhancement mode device, such as an enhancement mode MOSFET, which is the voltage at which the device begins to conduct.

2.3.2 History of MOSFET and Gan amplifiers

The development of GaN microwave transistors and MMICs (Monolithic Microwave Integrated Circuits) spans less than two decades from the first GaN-transistor demonstration to the beginning of industrial device implementation in electronic systems. GaN's potential as a high-power and high-frequency semiconductor transistor-based material was first recognized and explored in the early 1990s. The initial 10 to 15 years were focused on finding the best transistor constructions and making them reliable and stable. This stage was significantly supported by various research programs financed by military, governmental, and corporate bodies in the USA, Japan, and Europe, such as the Japanese program NEDO, the American DARPA programs WBGS-RF and NEXT, and European programs like KORRIGAN, UltraGan, Hyphen, and Great2 [14]

By the mid to late 2000s, leading electronic companies connected with the production of GaAs-components began investing in GaN technology. By 2006 and 2007, the market saw the introduction of the first commercial GaN-products, including universal wideband transistors with output CW power ranging from 5 to 180 Watt. Pioneers in the commercial market included Eudyna (now Sumitomo Electric Devices Innovation, SEDI), Nitronex, Cree, RFHIC, Toshiba, RF Microdevices (RFMD), TriQuint Semiconductor (TQ), and others. In 2009, TriQuint began producing ultra-wideband MMIC amplifiers with a bandwidth of 2 to 17 GHz. By the end of 2010, GaN-based transistors and MMICs were present in catalogs of over 15 companies globally [15]

Over the last decade, GaN technology has become increasingly important for RF applications. Its material properties enable devices with advantages in power density, form factor, breakdown voltage, thermal conductivity, operating frequency, bandwidth, and efficiency. Power amplifiers (PAs) are the predominant application for GaN devices, taking full advantage of these benefits. Strategy Analytics started tracking revenue in the RF GaN market in 2007, noting that defense agencies provided early funding for device and process development, with defense applications serving as early adopters. From 2007 to 2013, approximately 85% of all RF GaN device revenue came from defense applications [16] [17]

In 2013, the RF GaN market experienced a significant inflection point, with revenue growth increasing dramatically. Base station equipment manufacturers, particularly Huawei, became enthusiastic adopters of GaN technology for next-generation base stations. The deployment of 4G LTE capabilities in China and the subsequent emergence of 5G have been major drivers for commercial RF GaN revenue growth. GaN technology is particularly suited for 5G base station deployments, which was the biggest growth engine for commercial RF GaN revenue going forward. [16]

GaN's ability to complement established technologies like GaAs is helping accelerate its adoption in both defense and commercial applications. GaN is also helping to improve system performance in applications struggling to meet the upper power,

frequency, and efficiency requirements of next-generation systems. It is, therefore, becoming the go-to technology for new wider bandwidth, higher-frequency RF applications

2.3.3 Gan Theory of Operation

As mentioned before GaN HEMPT are depletion mode devices, which means that the device is normally ON when the gate source voltage is Zero ($V_{GS} = 0$). [18]

It is important to realize these 2 key points:

- A positive high drain voltage and a lower negative gate voltage is needed when working with GaN
- The bias sequencing for GaN must be conducted in a certain sequence even before the RF signal is applied to the circuit or else the device will be damaged.

For GaN, the correct bias sequences for powering up and down are as follows:

For turn on:

1. Apply negative pinch-off voltage (V_G) on the Gate. The Voltage level depends on the amplifier.
2. Apply operating positive Voltage in the Drain (V_D)
3. Adjust the Gate Voltage (V_G) to a less negative level until the operating current consumption is reached.
4. Apply RF.

For turn of:

1. Turn off the RF Signal.
2. Set Gate Voltage (V_G) to the Pinch Voltage
3. Set the voltage of the drain in 0 Volts.
4. Set Gate Voltage (V_G) to 0 Volt.

Since this is a relatively new technology, there are no discrete IC solutions that can control that process, leaving the designer to implement its own solution about controlling the bias sequencing, and to build the necessary fail safes that prevent out of sequence operation.

3 Existing bibliography.

The paper, "Automatic & Fail-Safe Biasing of GaN Transistors," [19] describes a fully automatic and fail-safe bias circuit for GaN transistors that requires only a single

positive voltage power supply. The paper also provides a detailed explanation of the circuit operation, time delay, rise/fall time measurements, noise suppression, and temperature compensation.

The paper begins by explaining that GaN HEMT transistors are depletion mode devices that require a negative voltage for the gate and a positive voltage for the drain. The paper states that it is critically important to supply a negative voltage to the gate before any positive voltage is applied to the drain; otherwise, the transistor will draw its maximum possible drain current from the supply, leading to excessive thermal dissipation and device burnout. To solve this problem, the paper introduces Integra Technologies' fully automatic and fail-safe bias circuit for GaN transistors that requires only a single positive voltage power supply.

The paper then provides a detailed explanation of the circuit operation, which includes two stages. In the initial phase, a negative voltage is applied to the gate of the GaN transistor so that when the drain bias is subsequently applied, the device will be biased at pinch-off, i.e., no drain current will flow, except for the finite leakage current of the transistor as specified in the transistor's data sheet. This phase is fully automatic and fail-safe and is controlled by the circuit. Integra refers to this circuit as a Gate Pulsing and Sequencing circuit (GPS circuit). In the second phase of operation, when the diode detects the presence of an applied RF pulse, the circuit sets the gate bias voltage to the value required to achieve the desired quiescent current IDQ, after which the transistor amplifies the RF signal. In the off period of the RF signal, the gate voltage returns once more to the pinch-off voltage. There are four important points to note about using this GPS circuit, which the paper discusses in detail.

The paper also explains that the GPS circuit has several advantages, such as reducing the amount of shot noise injected into the receiver during the RF-off period, improving the overall system efficiency, and requiring the user to supply only a single positive voltage to the test fixture. The paper provides a detailed description of the circuit's operation, including the use of a charge pump to provide a linear ramp-up of the drain voltage and a temperature compensation circuit to maintain a constant quiescent current over temperature.

The paper concludes by presenting time delay and rise/fall time measurements and showing that the circuit suppresses the output noise in the RF-off period by >30 dB for a 500 W GaN transistor biased with a quiescent current of 200 mA. The paper also references a study on the implications of using kW-level GaN transistors in radar and avionic systems, which provides additional information on the subject.

Overall, the paper provides a comprehensive and detailed explanation of Integra Technologies' fully automatic and fail-safe bias circuit for GaN transistors and its advantages. The paper also provides practical information on circuit operation, time

delay, rise/fall time measurements, noise suppression, and temperature compensation, which can be useful for researchers and engineers working in this field.

The application note "GaN HEMT Bias Sequencing and Temperature Compensation Circuit " [20]presents a bias sequencing circuit that is designed to be used with Wolfspeed RF GaN HEMT devices. The circuit is designed to prevent device failures by ensuring that drain voltage is not applied until a negative gate voltage is ready and the DC input voltage is above 16V. The quiescent current of the device can be adjusted using a potentiometer and the gate bias temperature compensation circuit can be enabled or disabled as needed.

The circuit topology includes a high voltage, low turn-on resistance P-channel power FET and a wide DC input low drop regulator with 100mA current capability to regulate the DC input to positive 5V that connects to the switch capacitor regulated voltage inverter's DC input. The inverter provides a -4.5V with 15mA current capability DC supply for the gate of the GaN RF transistor and a Negative Ready REG signal output for the drain DC power control.

Overall, the bias sequencing circuit presented in this application note appears to be a well-designed circuit for use with Wolfspeed GaN RF devices. The various safety features included in the circuit topology make it a reliable and efficient option for device operation. The information presented in this application note may be useful for researchers and engineers working with Wolfspeed GaN RF devices and looking to optimize their device performance.

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The paper “Autonomous Biasing Circuit for GaN RF Amplifiers” [21] The paper presents an autonomous biasing circuit solution for Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) devices in RF amplifier applications. GaN HEMTs are known for their advantages in power conversion and RF amplification applications due to their high operating frequency range, high reliability, and efficiency factors. However, these devices face challenges such as unstable operation at lower drain-to-source bias voltage and temperature-compensated gate bias requirements. The proposed circuit aims to address these challenges and provide a suitable autonomous biasing solution for GaN HEMTs.

The primary objective is to design a biasing circuit without using any programmable logic circuits, such as microcontrollers or microprocessors, and control electrical or timing parameters using only resistor and capacitor values.

The paper focuses on the turn-on sequence and divides the autonomous biasing system into functional circuit blocks, such as RF Detector, RF Switch, and Gate Bias. The RF Detector circuit is responsible for detecting the input signal and generating a logic switching signal to enable other sections of the biasing circuit. The RF Switch uses a PIN diode to switch RF signals, and the Gate Bias section controls the gate voltage V_GS.

The authors begin by discussing the background of GaN HEMTs, their commercial use, and their significance in RF amplifier applications. The paper highlights the importance of linearity in RF amplifiers, which is a prominent feature of power amplifiers. Non-linearity can lead to higher intermodulation distortions and increased noise figure parameters.

The proposed circuit is designed as an all-analog autonomous biasing solution without using any programmable logic circuit. The primary objective is to control any tuning of electrical or timing parameters using resistor and capacitor values alone. The circuit is simulated in LTspice, yielding measurable electrical parameters that could be considered for designing an ASIC biasing semiconductor chip for GaN devices.

In the autonomous biasing system, the design focuses on three main blocks: RF Detector, RF Switch, and Gate Bias. These are essential for automating the bias process and detecting the input signal.

RF Detector: This block is responsible for detecting the presence of an input RF signal and enabling the power amplifier section. The RF detector circuit uses a high-speed Schottky diode, a capacitor, and a resistor for RF detection and filtering. The rectified and filtered voltage is then compared with a threshold reference voltage in an op-amp comparator to generate a logic switching signal that enables other sections of the biasing circuit.

Gate Bias: This block is responsible for controlling the V_GS or gate bias in the circuit. The proposed base circuitry combines an RC voltage sweep generator and a voltage summing circuit. Components R1-C1 and R2 create a basic voltage ramp-up circuit, which is then buffered and fed to a voltage summing amplifier. The second input to the summing amplifier is a fixed negative voltage corresponding to the V_GS pinch-off voltage (in this case, about -5V). The output of the summing amplifier is used as the V_GS of the GaN device. When the RC ramp circuit is enabled, the voltage across C1 increases, eventually activating the GaN device.

RF Switch: This block uses a PIN diode (D2) as a series pass diode switching combination, providing switching isolation up to around 40dB. Resistor R3 completes the DC path for D2 to turn on, while L1 acts as an RF choke to prevent RF leakage to the DC rail. Capacitors C2 and C3 provide 50 Ω coupling impedance, with R4 serving as a dummy load for simulation purposes. The output of C3 feeds the gate of the GaN device (M1) in the actual circuit.

The simulation results show that the voltage across C1 starts building at the beginning of the simulation and takes around 2uS to swing to positive saturation voltage due to the response time and slew rate of the op-amp comparator. The RF signal switching response of the PIN diode is depicted, and although the difference in RF peak voltage is not significant due to the limitations of the spice modeling, the variation in the peak-to-peak voltage of the RF signal can be identified. The simulation results of the Gate Bias section show that the sweep voltage across C1 increases from 0V up to the applied positive voltage to R1, which is set to 24V in the current simulation.

Simulation results demonstrate that the proposed autonomous biasing circuit can attain the desired bias in less than 10ms, which is 30 times faster than the timings mentioned in earlier works. The paper concludes that the presented solution can effectively bias GaN HEMT devices in RF amplification applications while reducing complexity and response time.

4 Methodology

4.1.1 System description.

The focus of this thesis is the development and implementation of a Gallium Nitride (GaN) Power Amplifier Controller System. This system is designed to efficiently manage and control the operations of a GaN-based amplifier, which is crucial for high-frequency, high-power applications in areas such as telecommunications and electronic warfare.

Key components of this system include an RF signal generator, a GaN power amplifier, various power supply units, and temperature monitoring circuits. The system is engineered to provide precise control over the amplifier's operating conditions, ensuring optimal performance and stability. It features advanced monitoring mechanisms for voltage, temperature and VSWR, ensuring safe and reliable operation under various conditions.

4.1.2 Implementation Steps

To ensure and verify its functionality and effectiveness of the controller, a methodology should be followed which at each stage will checks the capability of the various parts of the system so that if the result is not satisfactory, to be able to determine the shortcomings, the mistakes or accidental omissions made during manufacture.

Due to the fact that electronics don't excuse mistakes, all the individual parts of the system will be simulated under various conditions to determine that that the component selection is correct and that the individual parts of the system behave as expected.

At the end the complete system will be simulated, again under various conditions to determine that the full system behaves correctly under all circumstances.

Then a PCB implementation will be designed and manufactured. The manufacturing consists of only the bare PCB board. This means that the actual assembly must be performed using the selected components.

A laboratory should be set up with all the necessary materials and tools required for construction. Except for the individual electronic components that make it up the system it will need cables, copper strips, soldering iron, adhesive tape, mounting base with flashlight, multimeter, cutters, wire strippers and other tools for electronic construction. They are also needed devices such as desktop power supply, spectrum

analyser, oscilloscope, RF generator, microscope to examine the assembled pcb for defects, as well as a thermal / infrared camera, to examine the temperature raise of various components.

The design steps will be the following.

- First the design requirements will be set for the amplifier controller,
- A suitable amplifier will be selected.
- Suitable components for the negative voltage generation will me selected and they will be simulated.
- A way to monitor that the negative voltage is on the correct level will be design and simulated.
- Suitable components for controlled application of the operating voltage to the amplifier drain will be selected and then simulated.
- A way to set the negative voltage to the operating voltage will be designed and simulated.
- A way to switch set the negative voltage automatically open the application of the operating voltage in the drain will be examined and simulated.
- The temperature compensation circuit will be designed and simulated.
- The temperature monitoring circuit will be designed and simulated.
- Auxiliary power will be added for powering various leds and status indicators on the board.
- The complete system will me simulated under various conditions.
- A Separate system will be created for the monitoring of the VSWR and will raise an alarm when a critical ratio has been reached.
- The above system will be simulated.
- The pcbs will be designed and manufactured.
- The pcbs will be assembled and examined for defects.
- The pcbs will be powered on and all the individual features will be examined with the use of an oscilloscope.
- Finally the pcbs will be connected with an amplifier to verify that indeed everything works as expected.

4.1.3 Simulations.

For the Simulations of the components, a SPICE [22] (Simulation Program with Integrated Circuit Emphasis) compatible simulator called LTspice will be used.

It is not practical to breadboard integrated circuits before manufacture, and in the case of SMD components (surface mount) its impossible. Considering the fact that every change requires manufacturing a new pcb then waiting for it to be shipped from

China, it is essential to design the circuit to be as close to perfect as possible before the integrated circuit is first built. Simulating the circuit with SPICE is the industry-standard way to verify circuit operation at the transistor level before committing to manufacturing an integrated circuit. [23]

Even with a breadboard, some circuit properties may not be accurate compared to the final printed wiring board, such as parasitic resistances and capacitances, whose effects can often be estimated more accurately using simulation. Also, designers may want more information about the circuit than is available from a single mock-up. For instance, circuit performance is affected by component manufacturing tolerances. In these cases, it is common to use SPICE to perform Monte Carlo simulations of the effect of component variations on performance, a task which is impractical using calculations by hand for a circuit of any appreciable complexity.

Figure 4. LtSpice Logo

LTspice provides schematic capture to enter an electronic schematic for an electronic circuit, an enhanced SPICE type analog electronic circuit simulator, and a waveform viewer to show the results of the simulation. Circuit simulation analysis based on transient, noise, AC, DC, DC transfer function, DC operating point can be performed and plotted as well as Fourier analysis. Heat dissipation of components can be calculated and efficiency reports can also be generated.[citation needed] It has enhancements and specialized models to speed the simulation of switched-mode power supplies (SMPS) in DC-to-DC converters.

LTspice does not generate printed circuit board (PCB) layouts, but netlists can be exported to PCB layout software. While LTspice does support simple logic gate simulation, it is not designed specifically for simulating logic circuits.

It is used by many users in fields including radio frequency electronics, power electronics, audio electronics, digital electronics, and other disciplines.

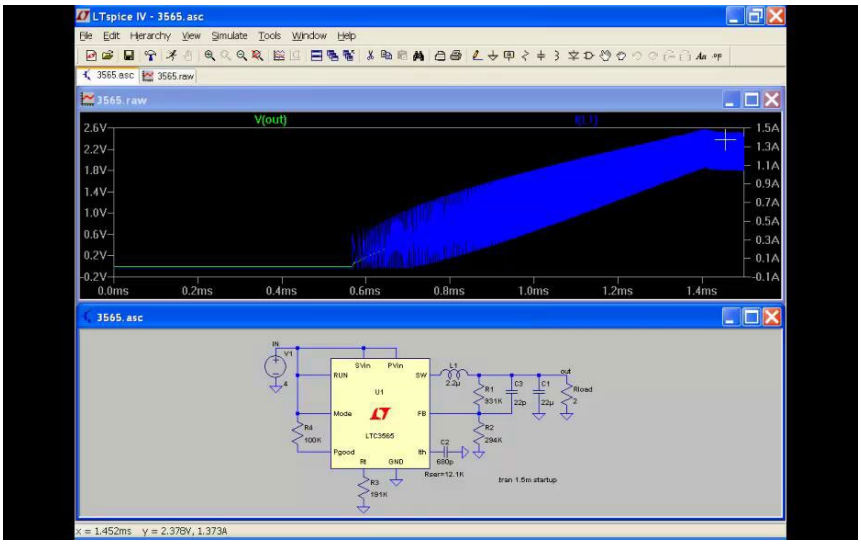


Figure 5. Lt Spice working environment

5 Implementation.

5.1 Design Requirements

To design a generalized amplifier driver for GaN, many design requirements must be taken into account. For this implementation the following design requirements will be implemented:

- The ability to drive a minimum of 30W Gan amplifier. This will give a lot of versatility to the driver so that it can be used on many different applications and with different power requirements.
- Ability to generate all power from a single voltage internally. Having a device that requires multiple power supplies to operate is usually problematic and complicates the supporting circuits. This means the following: 50V enters and is converted to -XV via an inverting DC-DC Converter. Additionally a 3.3V is generated from a buck converter to conform to any auxiliary power requirements.
- Adjustable negative voltages for the ability to drive different models of amplifiers. Some low power amplifier require -3 to -5 VGS, while other amplifiers of higher power (25W+) require -8 VGS. The ability to have adjustable negative voltages, gives again versatility to the driver.
- Overvoltage and undervoltage protection
- Overcurrent and short circuit protection.
- Automatic power sequencing with failsafes. It should be impossible for voltage to be applied to the Drain without the correct Pinch Voltage to be applied to the Gate.
- Automatic sequencing for Power Loss. The automatic sequencing shouldn't fail on sudden power loss.
- Temperature Compensation. The internal resistance of the amplifier substrate changes with the junction temperature. As a result, the gate voltage must be adjusted a tiny amount (at the order of 0.5mV per °C) depending the junction temperature
- Temperature Monitoring. The driver must have the ability to monitor the temperature of the amplifier, and raise an alarm at a critical voltage. On overtemperature alarm will not automatically shutdown the amplifier because an additional microcontroller that controls the RF application must turn off the RF before shutting off the power to the amplifier.
- Vswr Protection and Alarm. The driver should include an additional protection for VSWR (Voltage Standing Wave Ratio). When Rf signals are injected to the amplifier, the output of the amplifier be connected to an antenna, or an equivalent load. If it is not, all the injected power will be reflected back to the

amplifier and will destroy it in a few milliseconds. The driver should have the ability generate an alarm if an rf signal is injected without a load connected.

5.2 Component Selection

5.2.1 RF Signal Generator

An RF generator from Vaunix has been selected for generation of the RF signal.

Figure 6: RF Signal Generator

Vaunix LSG and LMS Series Lab Brick RF and Microwave USB Programmable Digital Signal Generators offer high output levels and excellent spectral purity through 40 GHz. They can be operated in both continuous-wave (CW) and swept-frequency modes. These ortable, USB powered, hand-held wireless signal synthesizers and programmable synthesizers are ideal wireless testing devices for engineering and production test laboratories, field wireless testing, and integration into high speed automatic-test-equipment (ATE) systems. They've been proven effective as portable local oscillators (LO) sources, RF test equipment microwave and for wireless testing applications.

5.2.2 HMC8205 0.3 or 0.4 GHz to 6 GHz, 35 W, GaN Power Amplifier

The HMC8205BCHIPS is a gallium nitride (GaN), broadband power amplifier that delivers 45.5 dBm (35 W) with 40% power added efficiency (PAE) across an

instantaneous bandwidth of 0.4 GHz to 6 GHz. No external matching is required to achieve full band operation. No external inductor is required to bias the amplifier. In addition, dc blocking capacitors for the RFIN and RFOUT pins are integrated into the HMC8205. The HMC8205BCHIPS is ideal for pulsed or continuous wave (CW) applications, such as military jammers, wireless infrastructure, radar, and general-purpose amplification.

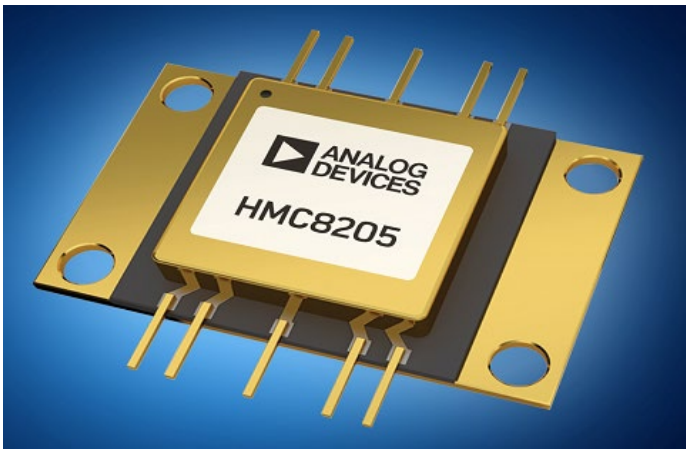


Figure 7. Selected GaN Amplifier

To avoid the need to manufacture an expensive pcb, an evaluation board of the above device is used with a part number EV1HMC8205BF10

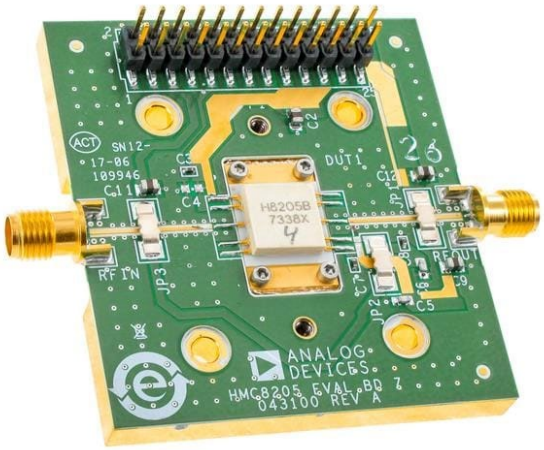


Figure 8: GaN Amplifier Evaluation Kit

The EV1HMC8205BF10 evaluation board is a two layer PCB fabricated using 10 mil thick Rogers 4350B copper clad. The PCB is mounted to a copper heat spreader which assists in providing thermal relief to the part as well as mechanical support to the PCB. Mounting holes allow for easy attachment to larger heat sinks for improved thermal management. The RFIN and RFOUT ports are populated by 2.9 mm female coaxial connectors and their respective RF traces have a 50 ohm characteristic impedance. The board is populated with components suitable for use over the entire Operating Temperature range of the part.

This amplifier requires 50V operating voltage and -8V Gate voltage.

5.2.3 ADL5519 1 MHz to 10 GHz, 62 dB Dual Log Detector / Controller.

The ADL5519 is a dual-demodulating logarithmic amplifier that incorporates two AD8317s. The AD8317 is a demodulating logarithmic amplifier, capable of accurately converting an RF input signal to a corresponding decibel-scaled output. The ADL5519 provides accurately scaled, independent, logarithmic output voltages for both RF measurement channels. The device has two additional output ports, OUTP and OUTN, that provide the measured differences between the OUTA and OUTB channels. The on-chip channel matching makes the log amp outputs insensitive to temperature and process variations. The dual logarithmic amplifier can be used to find the current input and output power ratio, ie in simpler terms in can be used to detect fatal VSWR.

5.2.4 Lab power supply

Voltage-regulated power supplies are necessary equipment in scientific and technical laboratories. They provide an adjustable, regulated source of electrical power to test circuits under development.

A generic Lab power supply that is able to provide 50V DC (and 5A) has been selected.

Figure 9. Lab Power Supply

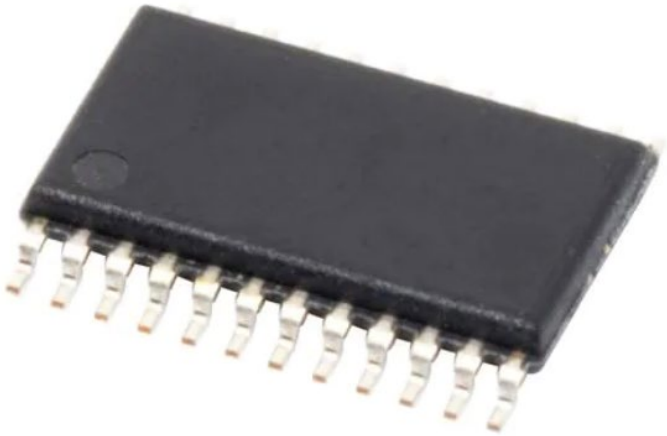
5.2.5 Positive High Voltage Hot Swap Controller LTC4260

A hot-swap controller is a circuit or device that is designed to safely allow the insertion or removal of electrical components, such as printed circuit boards or storage drives, from a system while it is powered on. Hot-swap controllers are commonly used in computer systems, data centers, and other electronic systems where it is necessary to be able to add or remove components without powering down the entire system.

Hot-swap controllers are used to manage the inrush current that occurs when a component is inserted into a live system and to protect the component and the system from damage due to overvoltage or overcurrent.

In general, hot-swap controllers are used to improve the reliability and uptime of electronic systems by allowing components to be added or removed without the need to power down the entire system. This can save time and reduce downtime in critical systems that require high availability.

To control the application of operating voltage to the amplifier a hot swap controller from linear technologies have been selected.



Moreover, it offers some additional features like:

- short circuit protection,
- power monitoring,
- The ability to signal that the power is OK.
- The ability to use an inexpensive N-channel MOSFET (ie, a low side switch), to simulate a hide side switch (MOSFET).

5.2.6 Inverting DC/DC Controller LTC3863

An inverting DC-DC controller is a type of circuit or device that is used to control the output of a DC-DC converter that produces an inverted output voltage. A DC-DC converter is a type of power supply that converts a DC input voltage to a different DC output voltage, and an inverting DC-DC converter is a type of converter that produces an output voltage that is opposite in polarity to the input voltage.

An inverting DC-DC controller is used to regulate the output of an inverting DC-DC converter and to ensure that the output voltage stays within a specified range. The controller may use feedback from the output voltage to adjust the switching of the converter in order to maintain a constant output voltage.

Inverting DC-DC controllers are used in a variety of applications where it is necessary to produce an inverted DC voltage, such as in power supply systems, motor control systems, and battery management systems. They are commonly used to invert a positive input voltage to a negative output voltage or to invert a negative input voltage to a positive output voltage.

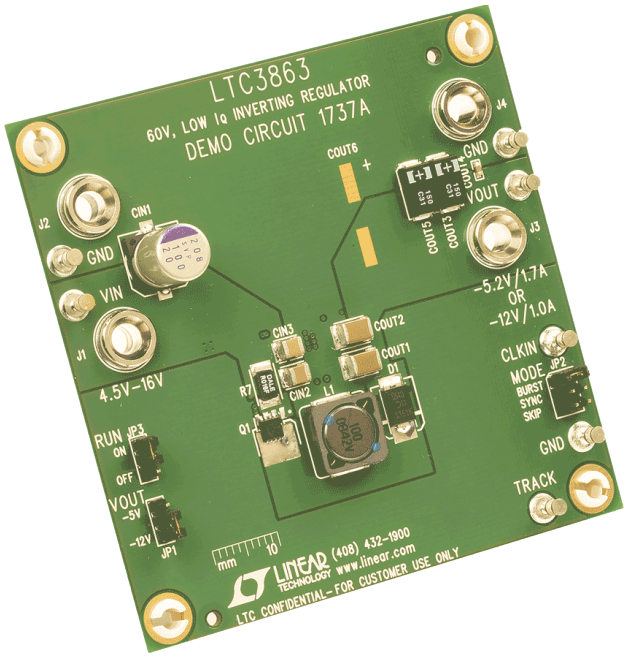


Figure 10: LTC3863 (Negative SMPS) evaluation board

For the Negative voltage generation LTC3863 has been selected which has a wide operating input voltage from (3.5 to 60V), and can output from -0.4V to -150V at up to 2A current. It should be more than enough to fulfil the gate requirements of any amplifier.

5.2.7 Negative Voltage Low Dropout Voltage Regulator. LT3015

An LDO regulator, or low-dropout regulator, is a type of linear voltage regulator that is designed to provide a stable, regulated output voltage from an input voltage that is slightly higher than the desired output voltage. LDOs are called "low-dropout" regulators because they can maintain a stable output voltage with a small difference between the input and output voltages.

LDO regulators are commonly used in battery-powered systems and other applications where it is important to minimize power loss and extend the life of the power source. They are also used in high-precision applications where it is important to maintain a stable and accurate output voltage.

LDO regulators are typically used to regulate a single output voltage, but some LDOs can be designed to regulate multiple output voltages. They are available in a range of output currents and output voltages and can be used in a variety of applications, including portable electronics, automotive systems, and industrial systems.

LDO regulators are generally simple to use and do not require complex external components, making them a popular choice for many applications. However, they do have some limitations, including a relatively low output current and a limited input voltage range, which may make them less suitable for some high-power applications.

While the inverting DCDC would be generally enough for the gate, there is an inherit problem with all the switching dc devices: they require filtering. To further decrease fluctuations on the gate voltage a LDO will be used in conjunction to “quiet” the voltage that goes to the amplifier gate. For that the LT3015 LDO from microchip has been selected.

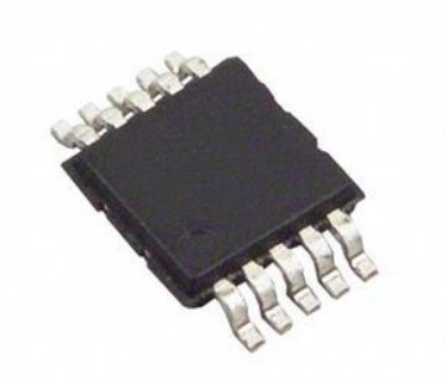
5.2.8 Dual Input Negative Voltage Monitor LTC2917

A voltage monitor IC, or integrated circuit, is a type of electronic device that is used to monitor the voltage of a power supply or other electrical system. Voltage monitor ICs are commonly used in a variety of applications, including power supply systems, battery management systems, and automotive systems, to ensure that the voltage in the system stays within a specified range.

Voltage monitor ICs typically have one or more input pins that are connected to the voltage source being monitored, and an output pin that provides a signal indicating the status of the voltage. The output signal may be a digital signal, such as a high or low voltage level, or an analog signal, such as a pulse width modulated (PWM) signal.

Voltage monitor ICs may also have additional features, such as programmable threshold voltages, built-in delay circuits, and multiple output configurations, which allow them to be customized for different applications.

In general, voltage monitor ICs are used to ensure the stability and safety of power supply and electrical systems by monitoring the voltage and providing a signal when the voltage exceeds a certain threshold. This can help to prevent damage to components and ensure the reliable operation of the system.



So, to ensure that no positive voltage will be applied to the amplifier, a negative voltage monitor from Linear Technologies has been selected.

5.2.9 Rail to Rail Operational amplifier LM7321

A rail-to-rail operational amplifier (op-amp) is a type of op-amp that is designed to operate with input and output voltages that span the full range of the power supply voltage. Rail-to-rail op-amps are commonly used in applications where it is necessary to amplify small signals with a wide dynamic range, such as in portable electronics and sensor systems.

Standard op-amps are limited in the range of input and output voltages that they can handle, and may not be able to amplify signals that span the full range of the power supply voltage. Rail-to-rail op-amps, on the other hand, are designed to operate with input and output voltages that are close to the power supply voltage rails, allowing them to amplify a wider range of signals.

Rail-to-rail op-amps are typically used in circuits where the input signal is small and the output signal needs to be amplified to a level that is near the power supply voltage. They are available in a variety of configurations, including single supply and dual supply, and can be used in a variety of applications, including signal processing, filtering, and amplification.

In general, rail-to-rail op-amps are useful in applications where it is necessary to amplify small signals with a wide dynamic range and where the full range of the power supply voltage needs to be utilized. They are a popular choice in portable and compact electronic devices where space and power efficiency are important considerations.

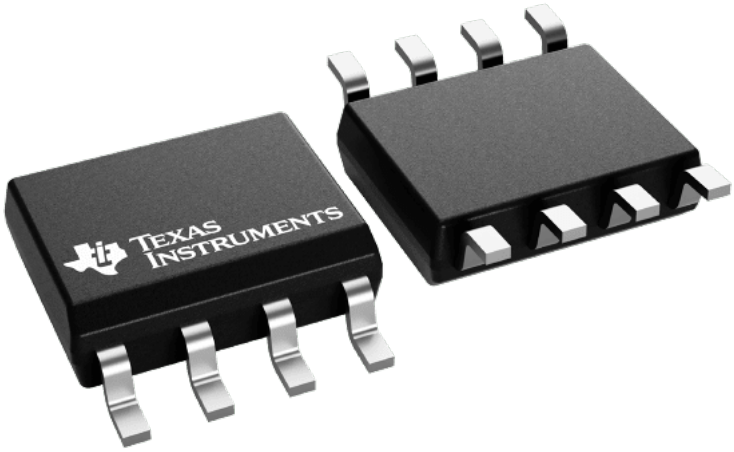


Figure 11: Rail to Rail OpAmp

In this case it an op-amp will me selected to set the operating negative voltage on the gate, and more specifically LM7321 from Texas instrument.

5.2.10 Step-Down Switching Voltage Regulator TL2757

For setting up the logic levels for the output pins, as well as for powering the auxiliary devices like leds, a simple step-down switching voltage regulator will be used. More specifically TL2757 from Texas instrument, which has the required support for 50V input.

5.3 Simulation Assumptions

There are some assumptions that need to be taken for the simulations.

First of all while SPICE simulations can be very useful for predicting the behaviour of a circuit or system under various conditions, they are not perfect and may not always accurately predict the real-world behaviour of a circuit.

There are a number of factors that can contribute to the accuracy of a SPICE simulation, including:

1. Model accuracy: SPICE simulations rely on models of electronic components and devices to predict their behaviour. These models may not always

accurately represent the real-world behaviour of the components, especially at extreme operating conditions or at high frequencies.

2. Circuit complexity: The complexity of the circuit being simulated can affect the accuracy of the simulation. Complex circuits with many components and interactions may be more difficult to model accurately, leading to a less accurate simulation.
3. Numerical precision: SPICE simulations rely on numerical methods to solve the equations that describe the behaviour of the circuit. These methods may introduce errors into the simulation, especially at high frequencies or when simulating nonlinear circuits.
4. Operating conditions: The operating conditions of the circuit, such as temperature, voltage, and load conditions, can affect the accuracy of the simulation. SPICE simulations may not accurately predict the behaviour of a circuit under extreme or unusual operating conditions.

Overall, SPICE simulations can be useful for predicting the behaviour of electronic circuits and systems, but it is important to keep in mind that they are not perfect and may not always accurately represent the real-world behaviour of a circuit.

Another assumption is that while the initial simulations are performed some components are assumed as ideal.

This simplification must happen both for time considerations (the simulations taks a long amount of time to complete), and practical issues (some parameters that are needed are not provided by the manufacturers in the first place).

This applies to the power suppliers which have no noise whatsoever and also on the resistors and capacitors, where any resistor capacitance is ignored, and any capacitors ESR is also ignored, except when it is absolutely necessary for the simulations (for example when examining the stability of the output of a simulated DC converter).

5.4 Power Input

The simulation assumes 50V power input from an external source.

For most of the simulations that voltage source starts at 0V reaches 50V then drops back down to 0V following the pattern of the following table.

Time (s)	Voltage (V)
0	0
0.01	0
0.05	50
0.2	50

0.22	0
0.25	0

An accurate model for the 3.3V step down back converter wasn't available for Ltspice, so the 3.3V was generated from another voltage source. Its activation timing was simulated using a SWITCH symbol that activates at around 3V Input, which is the same as the minimum operating voltage of the actual buck converter.

Finally a led status indicator is added to indicate that the power is in the board. The selected Led requires 2mA operating current, so a current liming resistor was added in series.

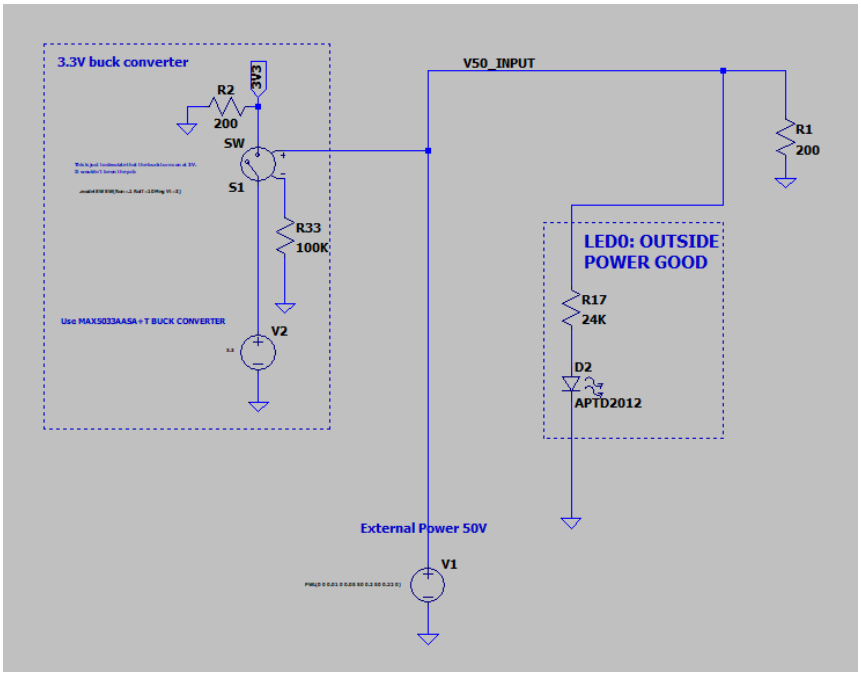


Figure 12. Power Input

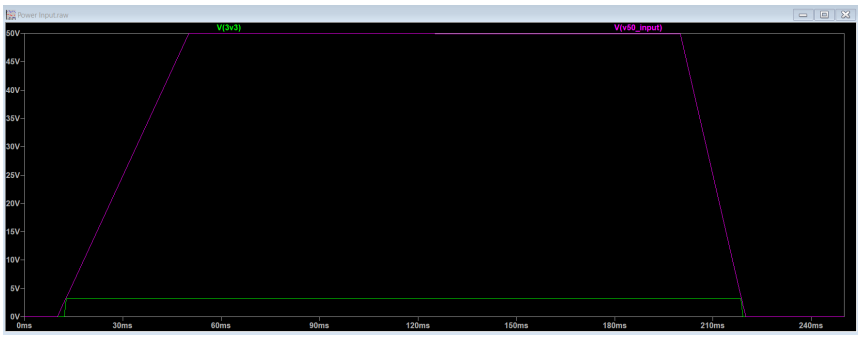


Figure 13. Power Cycle

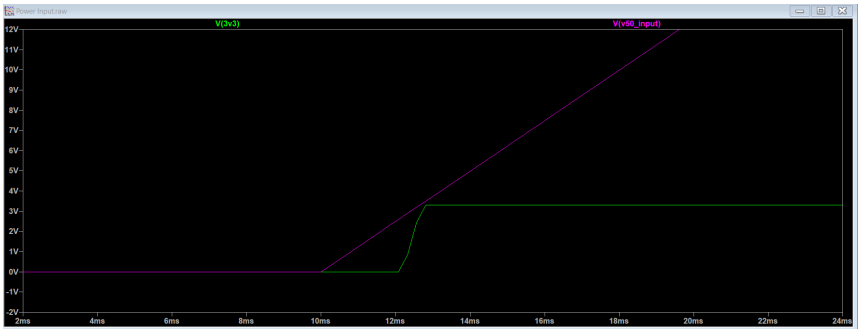


Figure 14. Buck converter Activation

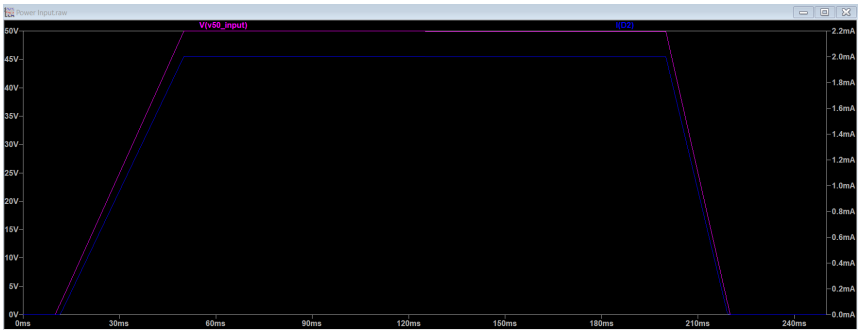


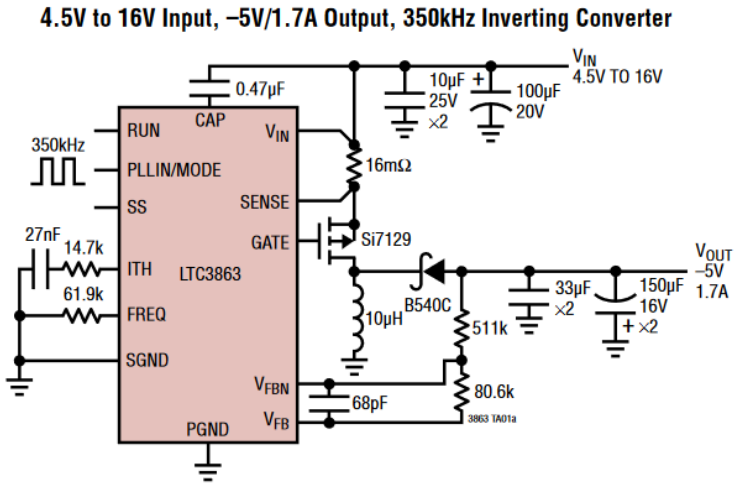
Figure 15. Led Power Consumtion

5.5 Negative Voltage Generation

5.5.1 Initial Negative Voltage Generation. DC/DC Inverter

For the first stage of the negative voltage generation LTC3863 has been selected which has a wide operating input voltage from (3.5 to 60V), and can output from -0.4V to -150V at up to 2A current. Unfortunately, is one of the most complex components in the system required additional care.

As always, it's a good practice to start with the typical application, even though most of the components will have to change.



5.5.1.1 Activation Threshold

For proper sequencing the whole sequence with the pinch voltage must ideally start when the external power has reached close to the minimum operating voltage of the amplifier (which is 28V). This can be accomplished by using the RUN pin on the LTC3863. The device starts when the RUN reaches 1.26V. It can be left floating, which will activate the device as soon as its minimum operating voltage has been reached, or it can be programmed by a carefully calculated voltage divider at that pin. The voltage divider equation is:

$$V_{out} = V_{in} * \left(\frac{R_2}{R_1 + R_2}\right)$$

And by setting activation voltage as 28V we get the following values for the resistors to breach the threshold of the 1.26V.

Activation voltage		
Vin	28	V

R1	100000	Ohm
R2	4700	Ohm
Vout	1.256924546	V

5.5.1.2 Operating frequency

The device supports 2 operating frequencies. 535kHz and 350Khz via the logic level on the FREQ pin. The 350Khz was selected by grounding the pin because even though higher bandwidth usually offers better performance, it also offers more switching noise which is harder to eliminate.

The minimum on-time required to generate -9V output from 50 V can be calculated with the following equation.

$$t_{ON(Min)} = \frac{(|V_{out}| + V_D)}{f * (V_{IN(MAX)} + |V_{out}| + V_D)} = 458.2ns$$

Where VD is the diode voltage drop.

The minimum tOn of the device is 220ns, so this is well within specs.

The capacitor on the CAP pin must be at least 0.1uF or 10X the Cmiller Capacitance of the Pchannel MOSFET. For it a .47uF ceramic capacitor was selected

5.5.1.3 Output voltage programming

The output voltage is programmed by connecting a feed back resistor divider from the output of the VFB PIN. The output voltage in steady-state operation can be set by the feedback resistors according to the equation

$$V_{Out} = -0.8V * \frac{R_{FB1}}{R_{FB2}}$$

To program as close as possible to –9V using standard resistor values we get the following values.

Setting Vout		
Vout	-8.96	V
RFB1	560000	Ohmn
RFB2	50000	Ohmn

Perfect voltage accuracy is not required since that task falls on the LDO later down the chain.

The integrator capacitor must be sized to encuse that the negative sense amplifier gain limits high frequency gain peaking in the DC/DC control loop. The minimum recommended value can be found with the following equation

$$C_{FB2} = \frac{1}{2 * \pi * 2 * R_{FB2} * FREQ_{SW}} = \frac{1}{2 * \pi * 2 * 50K * 350Khz} \approx 0.0454nF$$

5.5.1.4 MOSFET selection.

Extra care had to be taken when selecting the MOSFET because of the major difference of the Drain to Source Voltage (V_{DS}). Since the input voltage is 50V and the target voltage is -9V we have

$$V_{DS} = V_{CC} + |V_{out}| = 60V$$

So a MOSFET with a minimum of 70V V_{DS} Breakdown voltage must be used. The MOSFET is also able to switch on fast enough to accommodate that 450ns switching time.

Finally, no clamping of the gate voltage is required, because the GATE pin doesn't pull the voltage all the way to the GND so the MOSFET is not in any breakdown danger.

Considering the design requirements, the PMT200EPE was selected with conforms to all the specifications.

5.5.1.5 Inductor Selection

The inductor value must be selected so that the inductor ripple current is 60% of the average inductor current at maximum Vin and Full load. This can be found with the following equation.

$$L = \frac{V_{IN(MAX)}^2 * (|V_{out}| + V_D)}{0.4 * I_{OUT(MAX)} * f * (V_{IN(MAX)} + |V_{OUT}| + V_D)^2} = 159.7uH$$

Required inductor value.		
Vin	50	
Vout	-9	
Vd (diode forward conduction voltage)	0.5	
percentage	0.6	%
Maximum current	0.2	A
Frequency	350000	
inductor	0.000159728	H
	0.159727757	mH
	159.7277566	uH

The resulting current ripple can be calculated by the following equation.

$$\Delta I_L = \frac{V_{IN} * (|V_{OUT}| + V_D)}{L * f * (V_{IN} + |V_{Out}| + V_D)} = 0.053A$$

The inductor peak current can be calculated by the following equation.

$$I_{L(PEAK)} = \frac{I_{MAX} * \left(V_{IN(MIN)} + |V_{OUT}| + V_D\right)}{V_{IN(MIN)}} + \frac{\Delta I_L}{2} = 0.6A$$

Now that the inductance value has been determined, the type of inductor must be selected. Core loss is independent of core size for a given inductor value, but it is very dependent on the inductance selected. As inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore, copper losses will increase. High efficiency converters cannot tolerate the core loss of low cost powdered iron cores, so more expensive ferrite materials must be used. Moreover, to avoid excessive EMI generation from the switching, a shielded inductor must be selected.

5.5.1.6 Current Sensing and current limit programming

The RSense resistor value must be set to ensure that the converter can deliver the maximum peak inductor current with sufficient margin to account for component variastions and worst-case operating conditions.

Rsense can be calculated by the following equation

$$R_{SENSE} = \frac{95mV}{1.3 * I_{Peak}} = 0.25\ Ohmn$$

So anything less than that resistor will be enough to handle the peak current of the inductor.

5.5.1.7 Input and output capacitor selection

The input and output capacitance are required to filter the square wave current through the P-channel MOSFET and diode respectively. The selection of COUT is primarily determined by the ESR required to minimize voltage ripple and load step transients.

Multiple capacitors placed in parallel are needed meet the ESR and RMS current handling requirements. Tantalum capacitors will be ideal, but they have very low

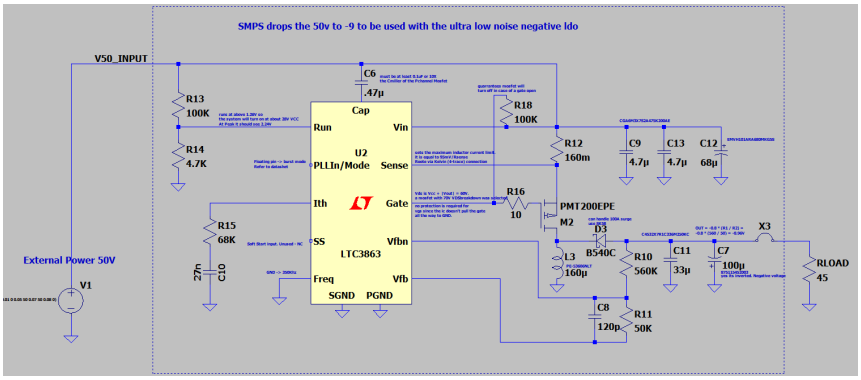
voltage and they tent to fail explosively if they are incorrectly selected. Ceramic capacitors would be the obvious choice but the high Q[2] of ceramic capacitors with trace inductors can also lead to significant ringing. To avoid this and dampen input voltage transients, a small electrolytic capacitor with low ESR will be used in parallel with the ceramic capacitors.

5.5.1.8 Fault Protection

The gate of the MOSFET should be pulled through a resistor to the input supply so that the P-Channel MOSFET is guaranteed to turn of in case of a GATE open.

5.5.1.9 Complete Schematic.

Considering the above design choices in the following image is the final schematic.



This is the resulting chart from the simulation.

We can see that the device activates correctly at 28V, it has the predicted inductor current, and reaches the target voltage without any oscillations.

[2] https://eepower.com/capacitor-guide/fundamentals/q-factor/#

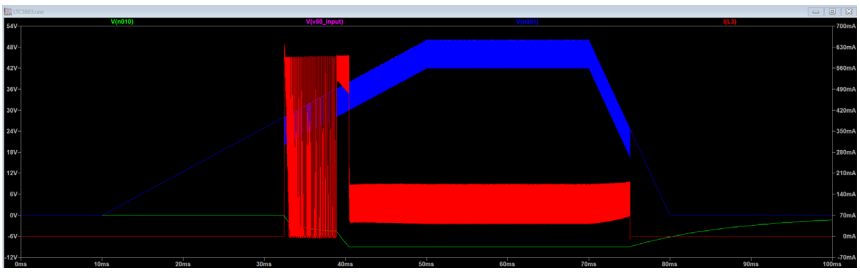


Figure 16. DC/DC inverter simulation

Figure 17. DC DC inverter activation at 28V

5.5.2 Second stage, stable negative voltage

As mentioned before, a switching DC/DC power supply has the disadvantage that its output will have unwanted noise. Under normal applications this doesn't have any negative effect, but since the amplification is controlled by that signal, it needs to be

as clean and as stable as possible before reaching the amplifier. To do this a LDO is used to drop the –9V voltage that was generated on the first stage to -8V.

The typical application circuit for the LT3015 is the following and it's a good place to start.

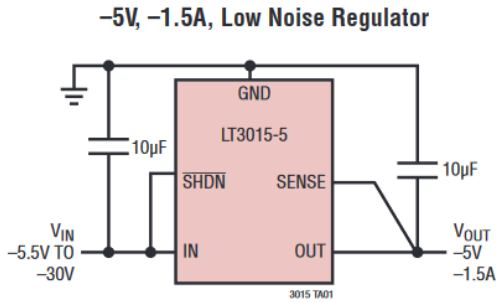
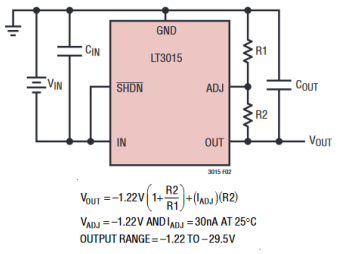


Figure 18. Typical application circuit

Since a specific voltage output must be reached, the adjustable schematic must be considered.



To calculate the output voltage the following equation must be used

$$V_{out} = -1.22 * \left(\frac{R2}{R1} + 1\right) + (I_{ADJ})$$

Using the above equation these values have been selected as a reference. While in this case a trimmer will be used to do the adjustment, it is a good practice to calculate the values as a referenc.

LT3015 Negative LDO voltage		
R1	4700	Ohmn
R2	26100	Ohmn
Iadj	0.000000003	A

Vout	-7.994893617	V

The LT3015 are stable with a wide range of output capacitors, but the ESR of the output capacitors affect stability, especially with small capacitors. So a minumem output capacitor of 10uF with an ERS of 500mΩ or less must be used to prevent oscillations. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes

In this case the thermally stable X capacitor is used with 0.1mΩ ESR.

Commented [GM1]: Add the value

For the verification a transient simulation of 1 second duration has been performed with the power in pulsing for 500ms

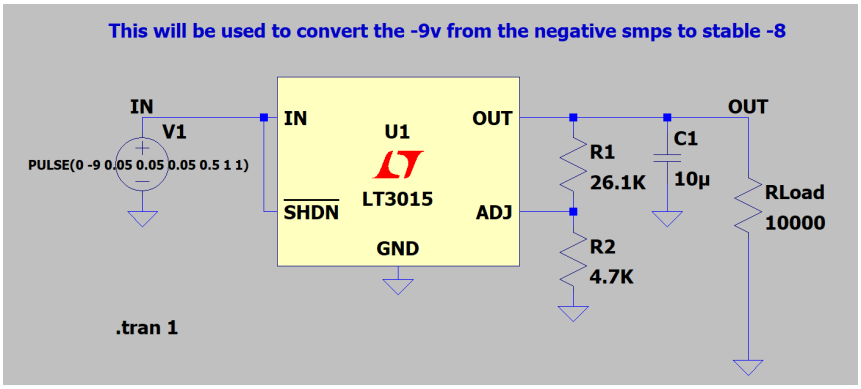


Figure 19. LDO LTspice simulation schematic

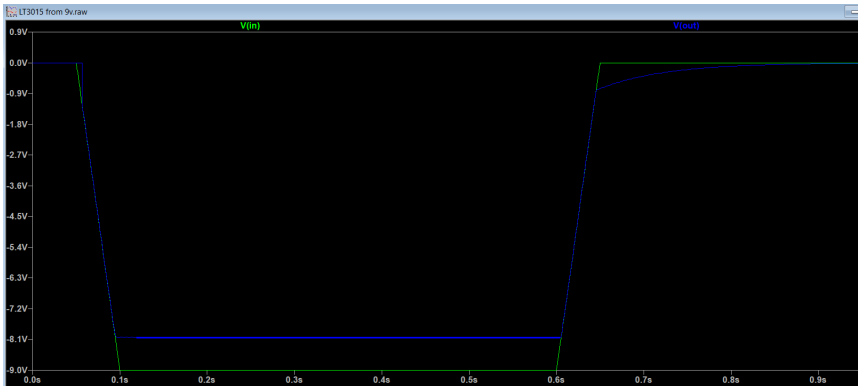


Figure 20. Simulation Result. System behaves as expected.

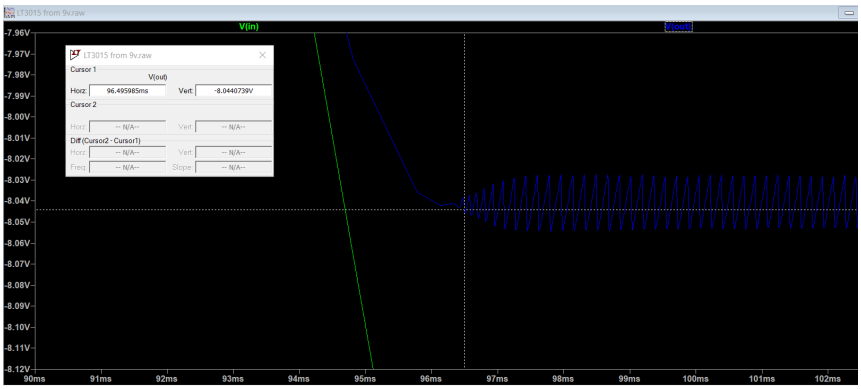


Figure 21. Close up on the target voltage.

After the simulation is completed, the results are satisfactory and as predicted from the datasheet.

The simulation can be found at `LT3015 Neg LDO\LT3015 from 9v.asc`

5.5.3 Negative Voltage monitoring

The LTC2919 is a voltage monitor that support negative voltages and can be configured to have Overvoltage and Undervoltage detection. The two adjustable inputs have a nominal 0.5V threshold, featuring tight 1.5% threshold accuracy over the entire operating temperature range. Glitch filtering ensures outputs operate reliably without false triggering.

The IC can be configured by setting the Logic Level on the SEL pin as appears in the following table.

ADJ1 INPUT	ADJ2 INPUT	SEL
Positive Polarity (+) UV or (–) OV	Positive Polarity (+) UV or (–) OV	V_{CC}
Positive Polarity (+) UV or (–) OV	Negative Polarity (–) UV or (+) OV	Open
Negative Polarity (–) UV or (+) OV	Negative Polarity (–) UV or (+) OV	Ground

In this application it will be set on the second option (Open) with -OV (overvoltage negative protection. The second monitoring will not be used.

The way that the system will be setup would be in such a way that anything between 0 to -7 volts will be registered as normal operating voltage. In that case the out1 pin will be in high impedance mode (open drain, or in other terms disconnected), and a

pull up resistor will pull the signal to 3.3V indicating that there is a problem with the monitored voltage.

Under -7 volts it will trigger the Overvoltage conditions and the OUT1 will be pulled to ground and become LOW. The reason that it has been setup the way its because that way the power good signal will be “BAD” by default. Only if the IC monitors the power correctly output can become LOW.

To minimize errors arising from the ADJ input bias and to minimize loading to the REF pin (which is used to drive the divider in negative applications), the Rn1 must be in the range of 5K to 100K.

The resistor values can be found with the following equation

$$R_{N2} = R_{N1}\left(1 - 2 * V_{Trip}\right)$$

And using a Rn1 of 6800 and Vtrip of -7, the rest of the values are:

Setting the trip voltage		
RN1	6800	Ohn
RN2	102000	Ohn
AdjX	-0.5	V
Vmon	-8	V
Vtrip	-7	V

For the simulation a transient simulation has been set with 2 seconds duration and a monitored voltage that goes under specifications 2 times.

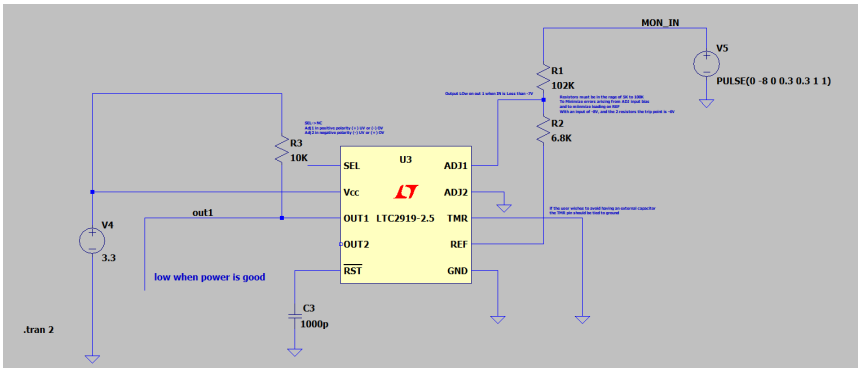
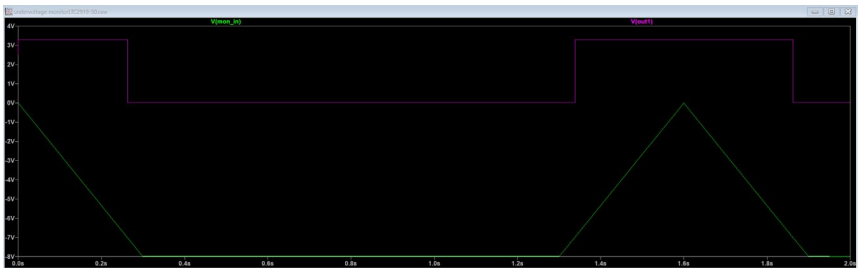
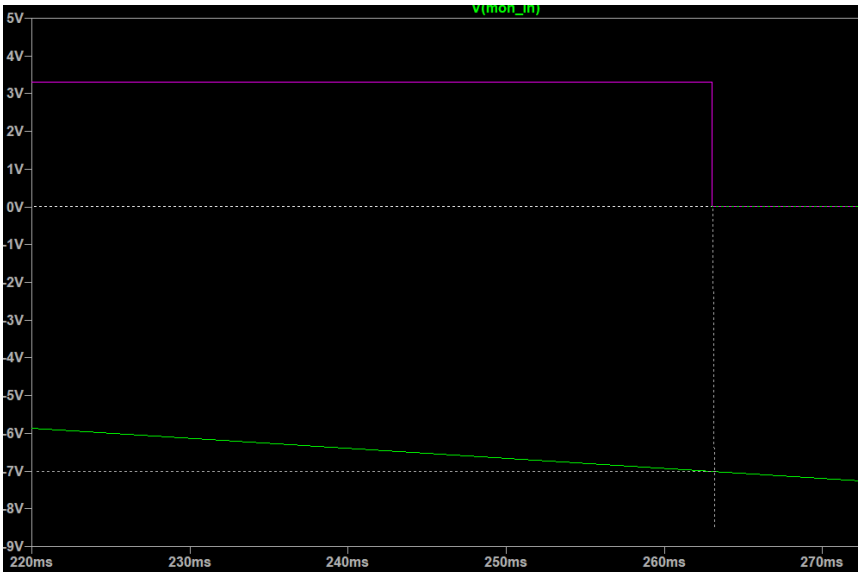


Figure 22. Negative Voltage Monitor Simulation.



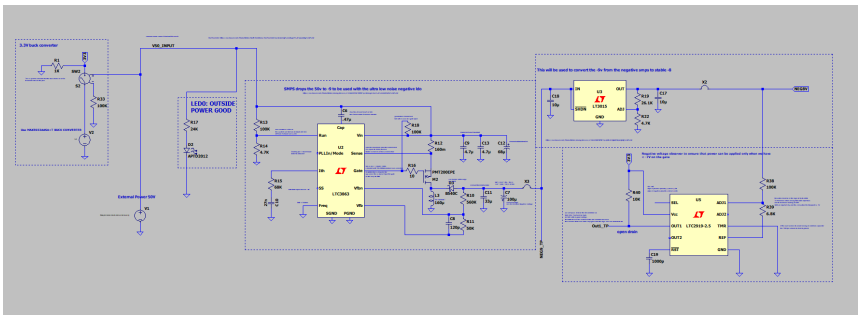
We can see from the simulation that the signal indeed goes low, only when the monitored voltage is less than -7 volts



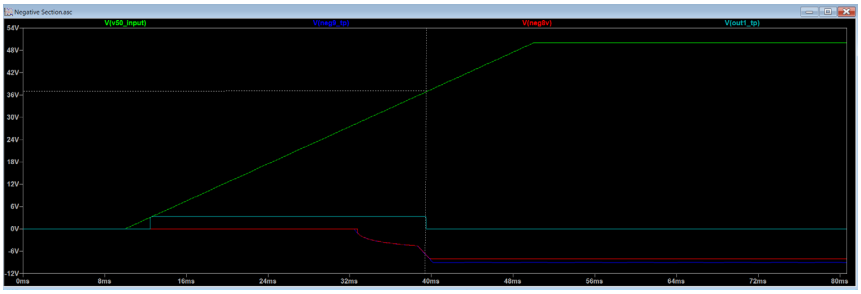
The simulation can be found as `LTC2919 Voltage Monitor`

5.5.4 Complete Negative Portion of the system.

The only thing remaining at this point for the negative voltage generation is to put all these 3 sections together to verify that they operate as expected.



The 50V external power is connected to the DC/DC inverter, which in turn has its output connected to the negative Ldo, and finally the output of the Ldo is monitored by the voltage monitor IC



- Greed line is the external 50V.
- Blue Line is the generated -9V
- Red line is the generated -8V
- And cyan line is the voltage monitor.

This is the result of the simulation. We can see that the sequencing works as expected up to this point.

The “Negative Power Bad” fault is registered as soon as the step-down buck converter activates.

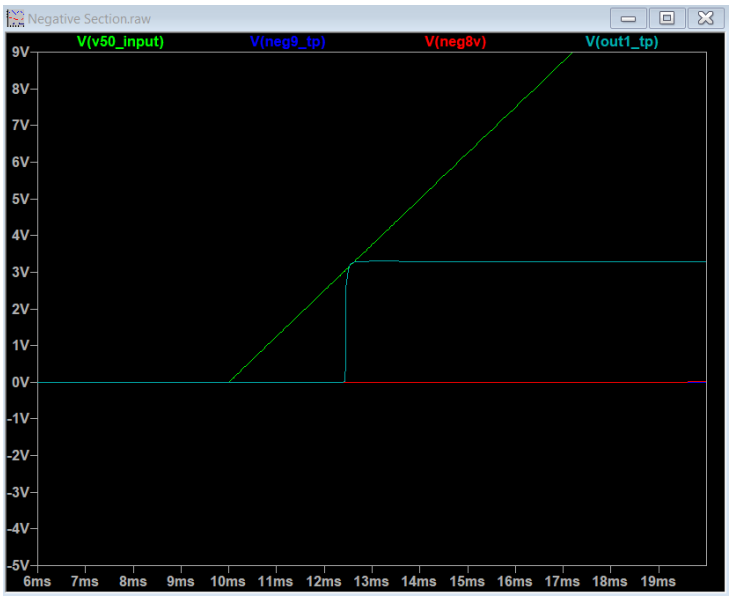


Figure 23. Negative Voltage Monitor Fault

And stays that way (HIGH) until at least -7V is reached from the LDO. At this point the external power is at around 40V.

Figure 24. Negative Voltage Fault has been released.

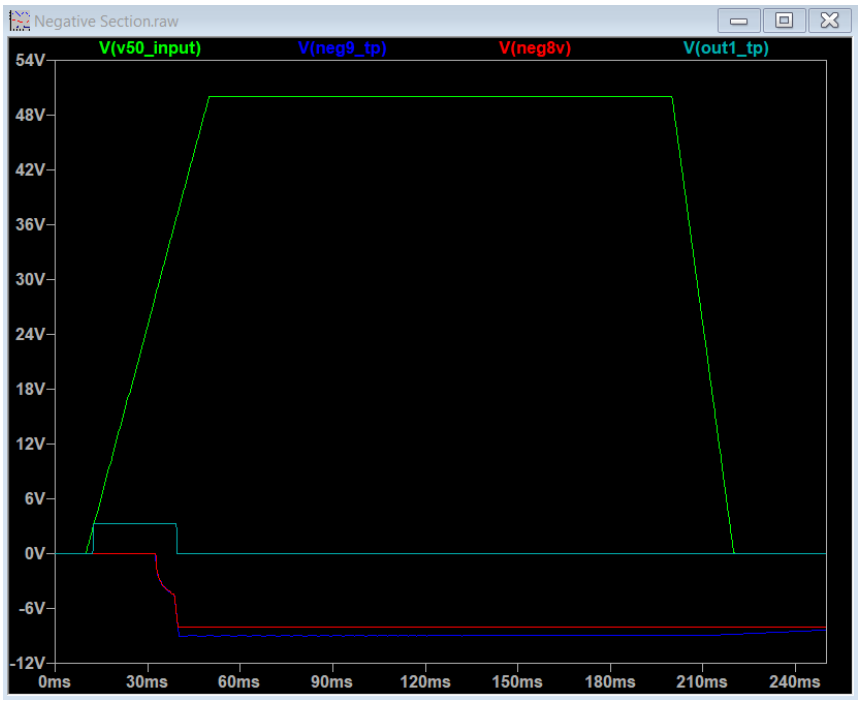


Figure 25: System Power Cycle

On power off the 50V drops to zero before the pinch voltage going to zero, as it should be.

5.6 Hot Swap Controller to power the drain

As mentioned before Hot-swap controllers are used to manage the inrush current that occurs when a component is inserted into a live system and to protect the component and the system from damage due to overvoltage or overcurrent. Besides that they offer many more advantages like the ability to use a N-channel switch for high side switching, and the ability to monitor the current that goes to the drain of the amplifier.

The selected IC (LTC4260) is very complicated and many calculations are needed for a successful application.

As always it is a good practice to start with the typical application and adjust accordingly.

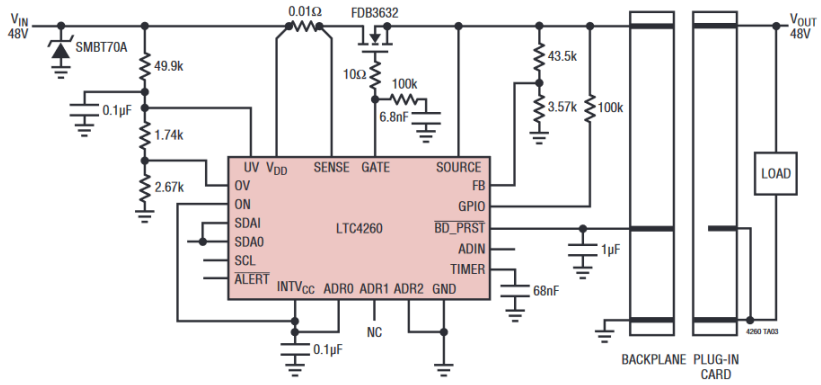
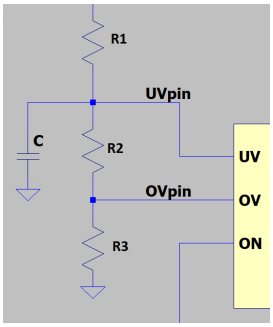


Figure 26. Hot swap controller typical application

5.6.1.1 Setting OV and UV.

The hot swap controller has an OV pin which monitors overvoltage and triggers an overvoltage fault if the voltage at this pin rises above 3.5V. It also has an UV pin which monitors undervoltage conditions and triggers an undervoltage fault if the voltage at this pin falls below 3.12V. This means that using two voltage dividers, the optimum operating voltage conditions can be set.

Instead of using 2 different voltage dividers a better solution, but slightly harder to calculate, is using a resistor network.



The voltage on the UV pin can be calculated with the following equation

The voltage on the OV pin can be calculated with the following equation.

$$V_{UVpin} = V_{in} * \left(\frac{(R_2 + R_3)}{R_1 + R_2 + R_3}\right)$$

$$V_{OVpin} = V_{in} * \left(\frac{R_3}{R_1 + R_2 + R_3}\right)$$

Using the following values

- Vin = 50V
- R1 = 68K
- R2 = 4.7K
- R3 = 4.7K

As well as the above equation the UV pin will see 6.07V and the OV pin will see 3.03V.

Solving the above equations as Vin using the Vov and Vuv thresholds we get respectively:

$$V_{ofUV} = \frac{3.12}{\left(\frac{(R_2 + R_3)}{R_1 + R_2 + R_3}\right)} = 25.7\ V$$

$$V_{ofOV} = \frac{3.5}{\left(\frac{R_3}{R_1 + R_2 + R_3}\right)} = 57.6V$$

The amplifier has an maximum operating voltage of 60V and minimum operating voltage of 25V, so resistor values are sufficient.

5.6.1.2 Selecting the Mosfet.

For the MOSFET PSMN5R0-80PS from experia has been selected. It offers 80 $_{VDSBreakdown}$ which is more than enough, 100A continuous operating current 270w Power dissipation and Rds On resistance of only 4.7mΩ.

A capacitor and a resistor are needed at the mosfet gate compensate the current control loop, and limit the inrush current. In this application that capacitor is named as slew rate capacitor. The voltage at the GATE pin rises with a slope equal to 18uA/C and the inrush current can be calculated with the following equation.

$$I_{INRUSH} = \frac{C_{Out}}{C_{SlewRate}} * 18uA$$

While under normal application the output capacitor should be fairly large, in this application a large capacitor will take a long time to discharge and may put the sequence of the amplifier activation out of order. As a result, for the initial design a 10uF capacitor is considered. For the slew rate capacitor was selected a capacitor to limit the inrush current to 1A.

With that in mind the above equation is:

$$I_{INRUSH} = \frac{10uF}{6.8nF} * 18uA = 1A$$

The time to change the capacitor can be calculated by the following equation

$$t_{CHARGUP} = \frac{C_L * V_{IN}}{I_{INRUSH}} = 19\ ms$$

The MOSFET must be sized to handle the power dissipation during the inrush charging of the output capacitor.

A MOSFET besides the normal operating current must be able to handle pulses of inrush current. This is called SOA (Safe operating area) curves and can be found on the datasheet. Considering the fact that in this case the InRush current is even less than the operating current of the amplifier this calculation is not needed.

The maximum operating current of the amplifier is 1.4A and the maximum peak current is 2.5A, so the maximum heat dissipation on the mosfet can be found using ohms law

$$P = R_{DSON} * I^2 = 30mW$$

To add some additional failsafes at the MOSFET, another small value resistor is needed at the gate to prevent high frequency gate oscillation, and the D1 Zener is used to clamp the Vgs to under the Vgsthres of the MOSFET.

5.6.1.3 Shunt resistor

This hot swap controller uses a Shunt resistor to monitor the current that is provided. Setting the current limit arbitrarily to 5.5A, the value of the resistor can be calculated with the following equation.

$$R_S = \frac{50mV}{I_{MAX}} = 10m\Omega$$

The power dissipation on the RS can be calculated to be 0.02W and 0.3W under normal operating conditions and at the current limit respectively, so a 0.5W resistor should be sufficient for all the operating conditions.

5.6.1.4 Feedback calculations.

The hot swap controller has a FB pin. A resistive divider from the output voltage is tied to this pin and when the voltage at this pin drops below 3.4V the output power is

considered bad and the current limit is reduced. Using the typical voltage divider equation, the resistors are selected so that any voltage under 40V is considered bad.

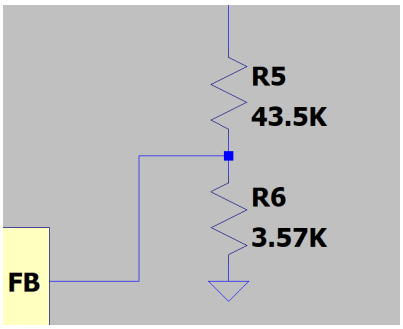
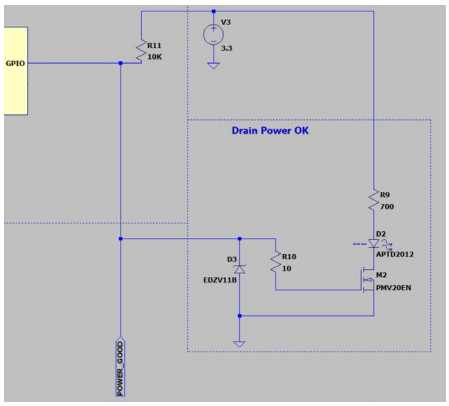


Figure 27: Voltage Divider Voltage Selection

5.6.1.5 Status indicators.

The Hot swap controller has a general purpose GPIO with open-drain logic output. It defaults to be pulled to GND to indicate that the power is bad. This means that this pin can be used to drive a status indicator led, as well as to be used a signal to indicate that the power is good downstream on the circuit.



5.6.1.6 Activating the hot swap controller

The Hot swap controller follows the following sequence:

First, the UV and OV pins must indicate that the input power is within the acceptable range and the PRST pin must be pulled low. All of these conditions must be satisfied for duration of 100ms to ensure that any contact bounce during insertion has ended.

When these initial conditions are satisfied, the ON pin is checked. If it is high, the external switch turns on. This mins that the controller can by activated by controlling the level of the ON pin.

5.6.1.7 Testing

The complete circuit can be found on the next image.

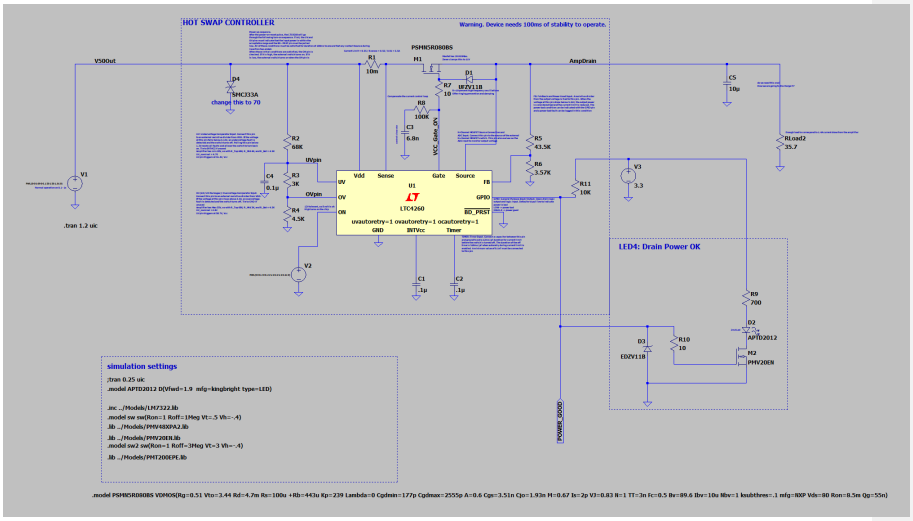


Figure 28: Complete Hot Swap Controller System

After the simulation we can see that the system behaves as expected.

After 100ms of stable operation the mosfet activates feeding power to the gate.

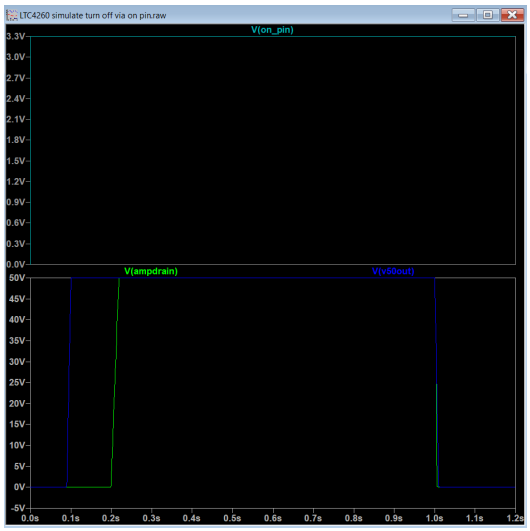


Figure 29: Activation after 100ms of stable operation

The same behavior can be seen controlling the ON pin level

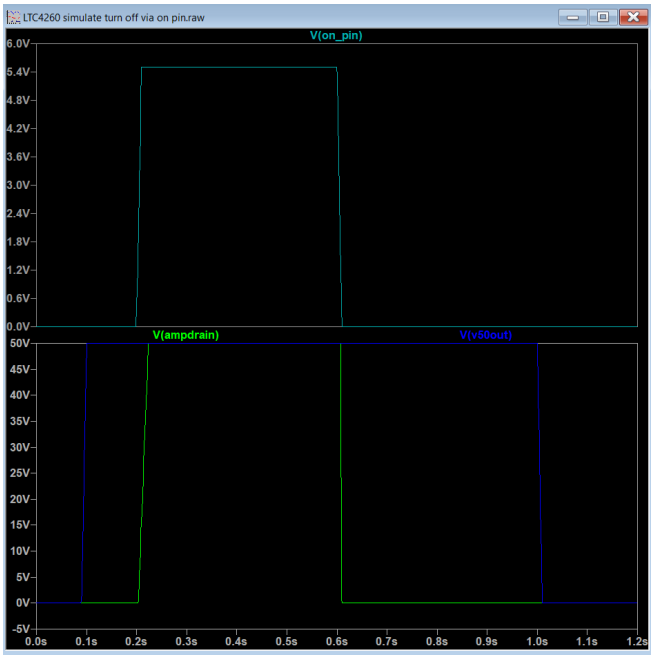


Figure 30: System Behavior on ON pin control

The POWER_GOOD indicator also works as expected.

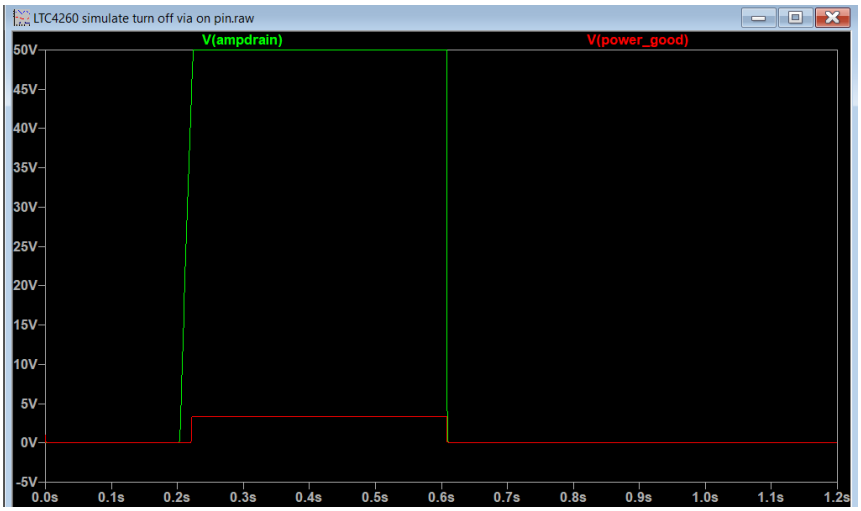


Figure 31: Behavior of "Power Good" Pin

Running the simulation without any connected load, the inrush current levels agree with the calculated values.

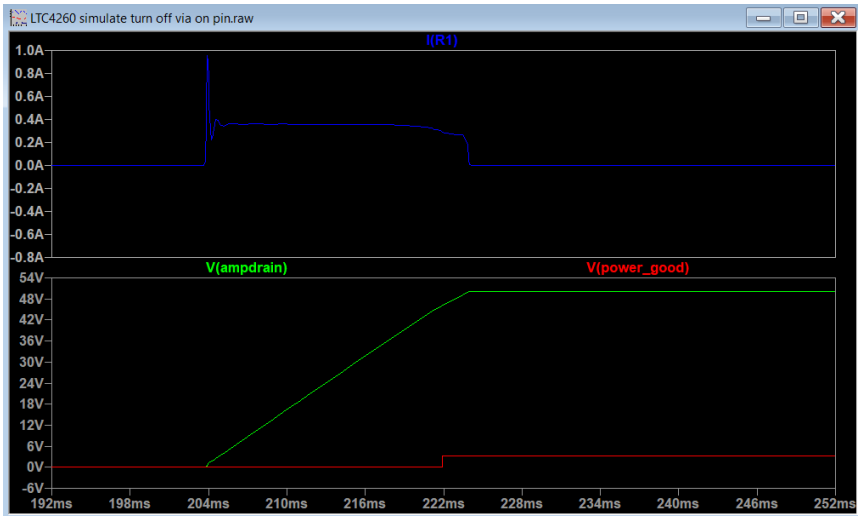


Figure 32: Blue Line indicates the inrush current behavior

Upon de-activation of the ON pin we can also see that the capacitors are discharging as expected.

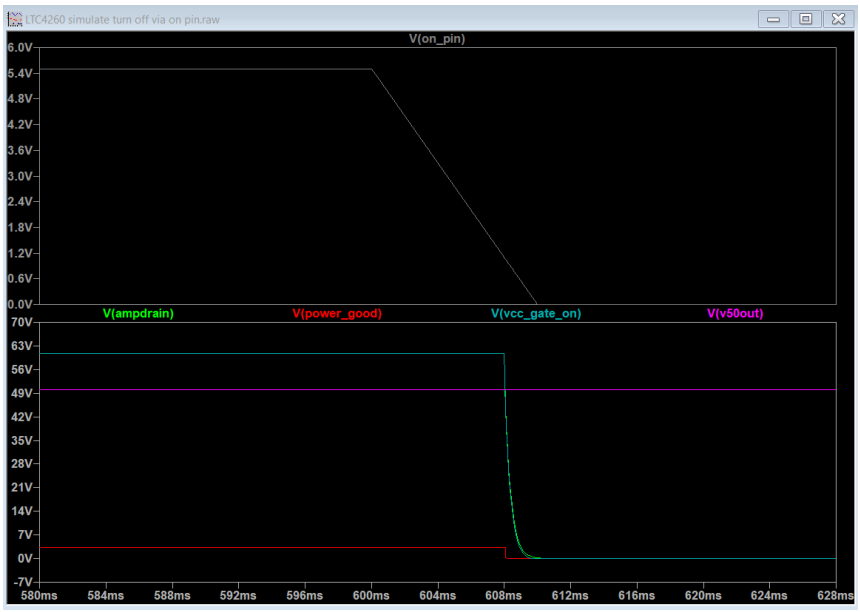


Figure 33: Capacitor Discharging

5.7 Current State of the circuit.

At this point most of circuit has been completed and can be put together and tested.

Since the negative voltage generation has been tested already and we have a signal to indicate that the negative voltage has been applied to the amplifier gate, we can use the signal from the voltage monitor to drive the ON pin of the hot swap controller. Of course, since the signal of the voltage monitor is LOW when power is good and the ON pin requires HIGH level to activate, the logic must be inverted using a simple MOSFET circuit

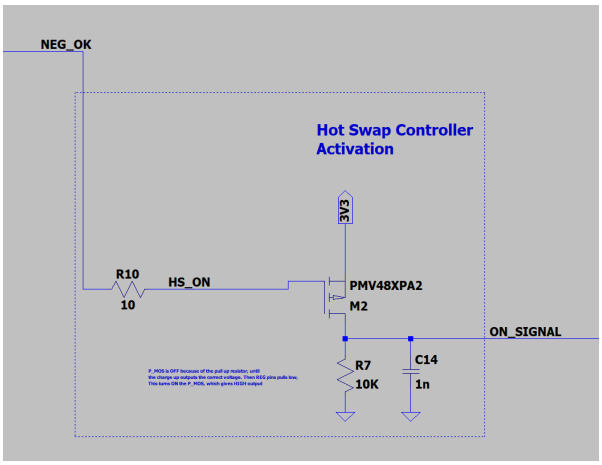


Figure 34: Using the signal from the voltage monitor to drive the ON pin of the hot swap controller.

The complete circuit can be seen in the following image.

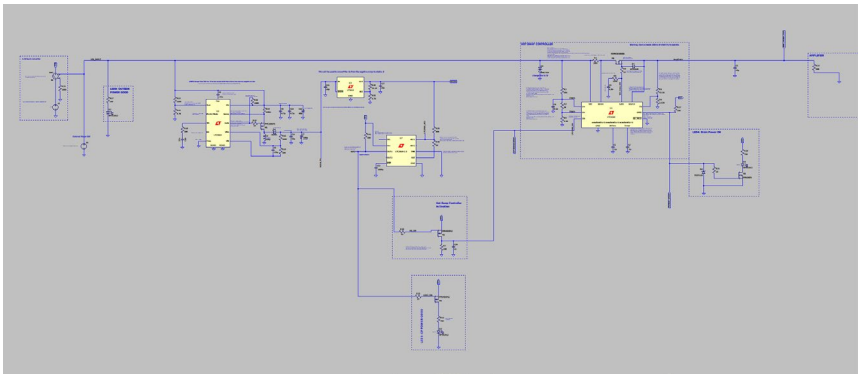


Figure 35: Complete Circuit at this time.

Running some simulations we can see that the sequencing up to this point behaves as expected.

5.8 Setting the gate voltage to the operating range

5.8.1 Getting the voltage to the target voltage

After the Drain has received the operating voltage (50V), the gate voltage has to be adjusted to around -2.4V. This can happen an any time as far as the above criteria is complete.

For this to happen a “signal” must trigger a sequence of events that will change the -8V to -2.4V.

There are multiple ways to get the signal, and each has advantages and disadvantages.

- Activating Automatically when the power sequence is complete. This is the best method since there is no way that the sequence will be performed out of order, but it has the obvious disadvantage that the amplifier will consume its full power independent if a signal is available or not.
- Using a button. The same as above, but it posses the danger that the amplifier will receive 50V on the drain without the gate voltage being at -8V. To avoid this additional circuitry must be implemented.
- Using a Logic High Signal from a microcontroller. Same issues as above.
- Using RF detection. The issue with that is that there is a measurable amount of delay from the RF detection until the signal generation. It is a small amount of time, but depending on the power level of the signal, RF power will reach the amplifier without the amplifier being fully active.

Whatever the case it is obvious that some additional circuitry must be added on the chain to avoid out of sequence activation. This will be addressed in a later chapter.

In any case, in its simplest form the actual switching to the target voltage (from -8V to -2.4V) can be performed using an op amp in a voltage follower mode with a voltage divider setup.

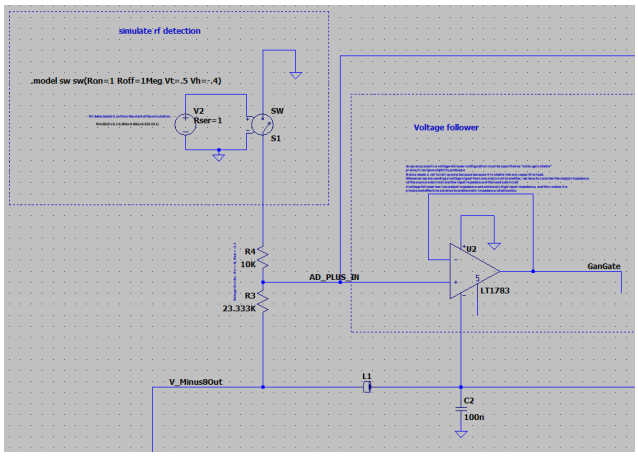


Figure 36. Negative Voltage adjustment

At normal operation the voltage follower will keep the voltage at -8 volt. When the power needs to go to -2.4V voltage (which is controlled by the R4 and R3 voltage divider), a "switch" is connecting the voltage divider on ground. In that case the

voltage follower acts as a comparator, and since the new voltage is less negative than the original voltage, it switches the voltage output to that target voltage.

The values of the Resistors can be found with the typical voltage divider equations and they are as follows:

Negative Voltage Divider		
Vin	-8	V
R1	23333.33333	Ohm
R2	10000	Ohm
Vout	-2.4	V

To have this adjustable a suitable trimmer will be used on the PCB.

The op-amp used in a voltage-follower configuration must be specified as “unity-gain stable" or else it can have stability problems. It also needs a rail to rail op amp because it is stable into any capacitive load. This whole conversion couldn't be done without any opamp because whenever a voltage signal is sent from one subcircuit to another, both the output impedance of the source subcircuit and the input impedance of the load subcircuit must be considered and matched. A voltage follower has low output impedance and extremely high input impedance, and this makes it a simple and effective solution to problematic impedance relationship.

On its own the voltage follower though is not enough and some additional circuitry is needed. Because the GAN quiescent gate current can increase at high temperatures, a significant voltage drop can be developmed accross this gate resistor, increasing Vgs by 200mV or more.
This can be a serious problem, because the increased gate voltage can put the operating point into a region of instability or even cause thermal runaway
One solution is to provide DC feedback from the gate terminal to the op amp inverting input, allowing it to compensate for voltage dropped across gate resistor.

To minimize RF non-linearity and memory effects, 1/(R x C) is less than the lowest modulation frequency of the RF signal. The final schematic of the op-amp can be seen in the next image

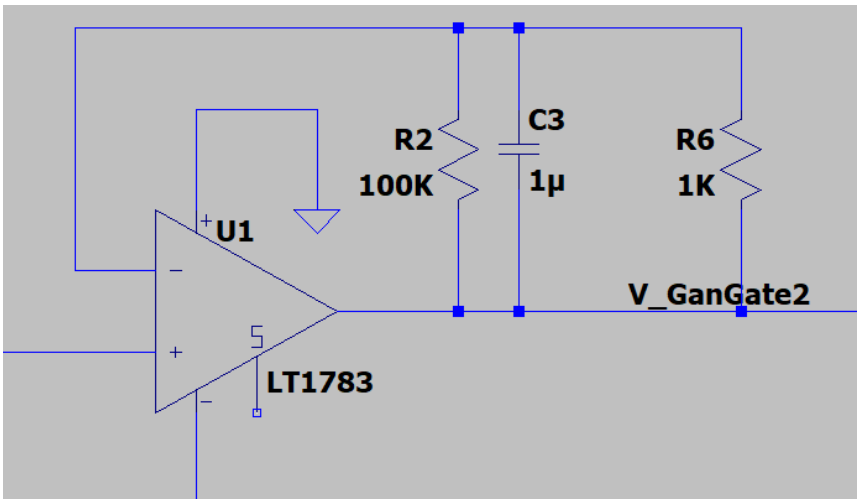


Figure 37: Voltage Follower OpAmp Schematic for the Gate Voltage

5.8.2 Switching the negative voltage

For the actual switching on the circuit, a negative voltage circuit has to be switched from a positive voltage.

This can be performed by a convoluted MOSFET topology and careful consideration of their threshold (V_{gstth}) and breakdown voltages ($V_{dsbreak}$).

Besides the complex design requirements, it also requires upwards to 15 extra components, making that solution impractical.

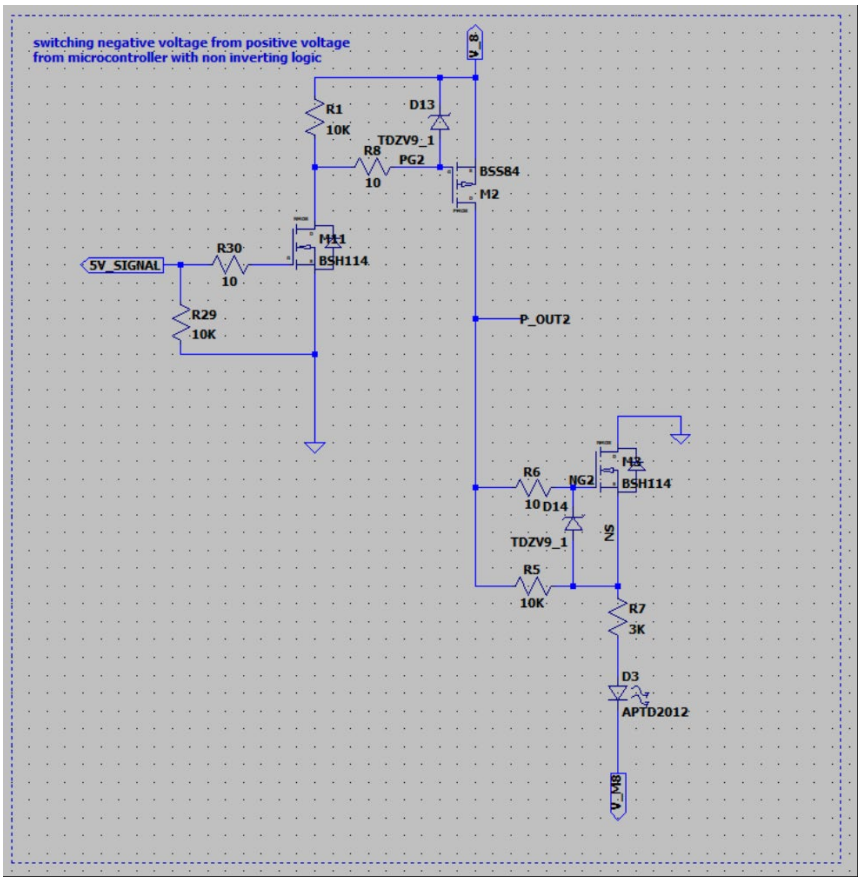


Figure 38. Switching negative voltages from positive voltage signal using MOSFETs

To avoid this complicated circuit, a better solution is to use a photo-MOSFET[3]. A normal optocoupler cannot be used for this application because it is used only for transferring signals.

For this application the photo MOSFET TLP241A was selected.

[3] Ie ,a low power solid state relay (SSR).

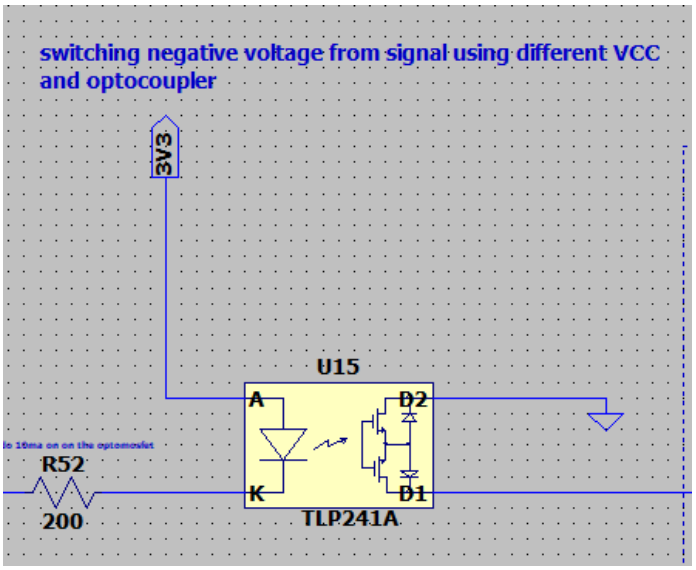


Figure 39: Using a photo-mosfet to switch on the negative voltage using positive voltage

The photo MOSFET requires 10mA operating current, so a suitable resistor must be added in series.

Photo MOSFET		
Supply Voltage	3.3	V
Led Type	Red	
Led Forward Voltage (Voltage Drop)	1.27	V
Desired Led Current	10	mA
Resistor	203	Ohm
Power Dissipation Led	0.0127	Watt
Power Dissipation Resistor	0.0203	Watt

In any case, for a versatile circuit it has been designed that it will over 3 ways of activation.

- Activating automatically, when the power sequence is complete.
- Using a button.
- Using a 3V signal from a microcontroller.

5.9 Adding Failsafes

To ensure that on power will reach the amplifier out of sequence, the signals from the hot swap controller and the negative voltage generation were added in series with the

signal that switches the negative voltage to enable the amplification. This ensures that the amplifier will never receive -2.4V at the gate without having already -8V at the gate and 50V at the drain.

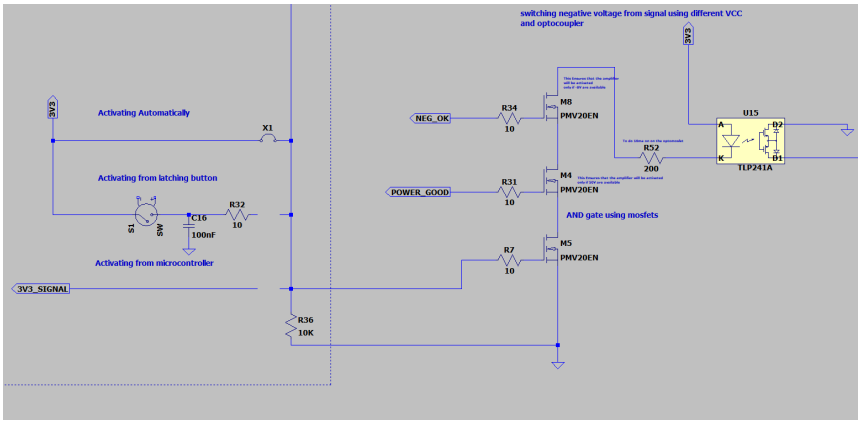


Figure 40: Addition of failsafes

5.10 Creating a simple amplifier model.

Unfortunately, there is not a model available for LTspice for that amplifier. There is also nothing available that can be used to approximate its behavior.

This issue can be solved by having a resistor in the simulation that changes in resistance depending on the AMP_GATE value. Basically, the amplifier behaves as a resistor with infinite resistance when the AMP_GATE voltage is at -8V and R = (50V/1.4A) when the AMP_GATE is -2.4V.

That behavior can be approximated with the following equation.

$$R_{amp} = \frac{V}{0.001 + \left((V * V_{Gate}) - (-8)\right) * \left(\frac{1.4 - 0.001}{-2.4 - (-8)}\right)}$$

This equation can be input directly into LTspice, and this is the resulting circuit

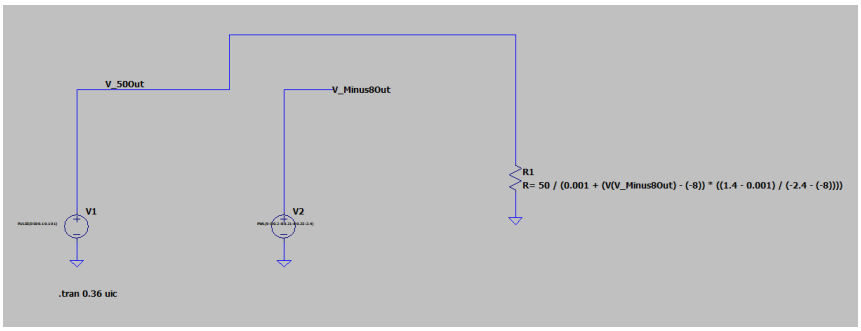


Figure 41: Amplifier model in LtSpice

After doing the simulation, the current draw of that resistor behaves exactly as expected

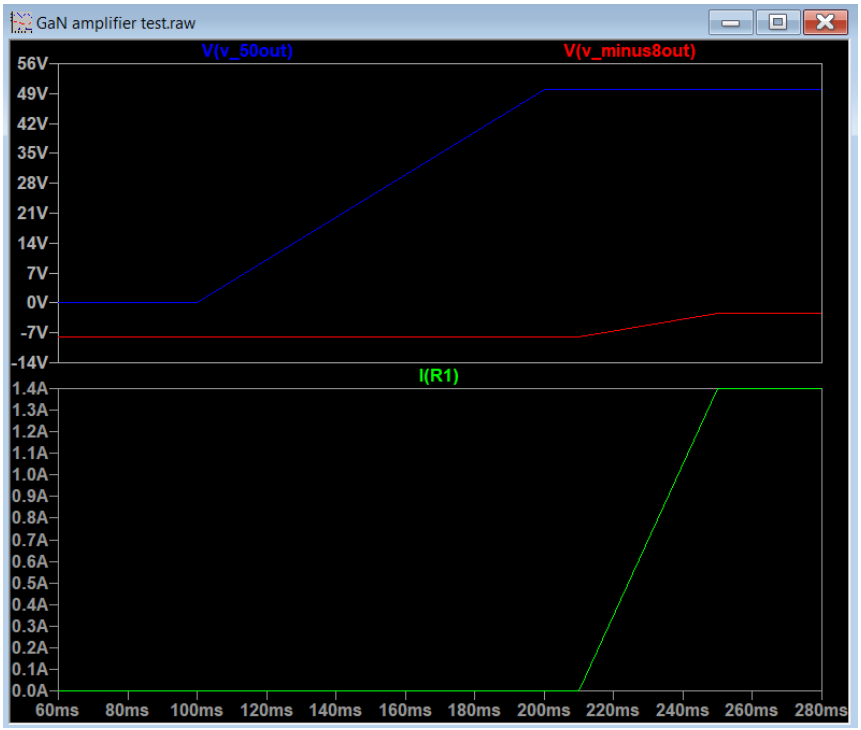


Figure 42: Verification of the behavior of the amplifier model

5.11 Designing the Temperature Compensation Circuit

The amplifier needs a complicated system to provide the temperature compensation voltage for the GaN amplifier. The internal resistance of the substrate changes as its temperature increases and the amplifier needs an adjustment of the gate voltage by about +0.6mV per °C to maintain constant current, and thus constant power.

On a normal amplifier, you would do the temperature compensation by placing the thermistor (with various resistors), after the opamp that controls the bias. This is not possible with this amplifier because it needs negative voltage at the gate, so everything is inverted.

In any case. as the temperature increases, the voltage has to be less negative and increase, so any thermistor in series has to be at the bottom portion of the resistor network, (ie closer to the ground), and it has to be NTC (Negative Temperature Coefficient) type. Also, since the circuit needs such a miniscule adjustment to the voltage a high initial resistance is needed; a normal 10K thermistor will be too low, and we need something like 500Kohn.

In the end a 470K NTC thermistor from Vishay was selected and more specifically NTCS0805E3474FXT.

Now, there are 2 different problems to solve. The first problem is the scaling of the thermistor. To make the circuit perform is needed, we need an input of around -4.8V, instead of -8V, so we need a circuit of nested voltage dividers. This would work, but this creates the second problem which is that since the nested voltage dividers work in unison, a disconnected or shorted thermistor will create an impedance mismatch and will completely move the divider output out of spec.

More specifically, a disconnected thermistor results in a -1.7V output voltage which will increase the drain current of the amplifier significantly and burn it.

To solve this, we need another voltage follower to fix the impedance issue and that stabilizes the voltage to -4.8 at the exit of the first voltage divider.

Now if the thermistor is disconnected the output voltage of the follower stabilizes to -2.42V.

If the thermistor is shorted, this will also burn the amplifier because it will guide the follower to 0V, so an additional 100K resistor must be added in series to the thermistor. The final result can be seen in the following image:

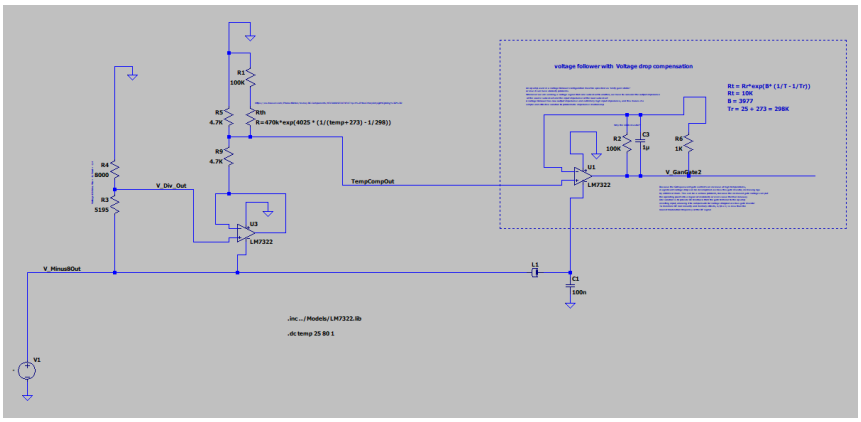


Figure 43. Complete Temperature Compensation Circuit without switching

The voltage divider generates the -4.8V.

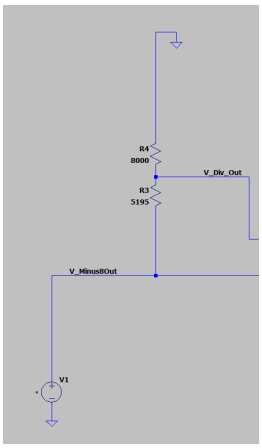


Figure 44. Voltage Divider of Temperature Compensation Circuit

Then it connected to the voltage follower with the thermistor and divider network.

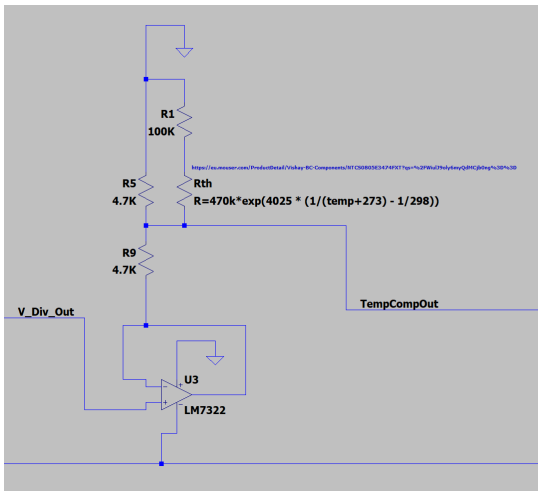


Figure 45. Resistor network.

The selected thermistor has a beta value of 4024 and its resistance and temperature relation can be found by the following equation.

$$R_{th} = 470K * e^{\left(b*\left(\frac{1}{(temp+273}-\frac{1}{298}\right)\right)}$$

The calculated values of the thermistor with the series resistor as well as the output of the voltage divider network can be found on the following table:

Base Thermistor Resistance	470000	ohmn
B value	4025	
Auxiliary Resistor	100000	ohmn

Temperature	Resistance	Voltage input	R1	R2	R2 + RTh (Ohmn)	Vout (V)	delta (mV)
25	570000	-4.8	4700	4700	4661.562554	-2.39015	
26	549241.1145				4660.122115	-2.38978	0.370855
27	529528.4384				4658.650648	-2.3894	0.378961
28	510803.2168				4657.148667	-2.38901	0.386943
29	493010.3136				4655.616753	-2.38861	0.394782
30	476097.9701				4654.055546	-2.38821	0.402464
31	460017.5802				4652.465754	-2.3878	0.409971
32	444723.4829				4650.84814	-2.38738	0.417289
33	430172.7679				4649.203533	-2.38696	0.4244
34	416325.0964				4647.532819	-2.38653	0.43129
35	403142.5338				4645.836939	-2.38609	0.437944
36	390589.3938				4644.116892	-2.38565	0.444348
37	378632.0943				4642.373727	-2.3852	0.450487
38	367239.0221				4640.608544	-2.38474	0.456348

39	356380.4082				4638.822491	-2.38428	0.461919
40	346028.2103				4637.016757	-2.38381	0.467189
41	336156.0046				4635.192575	-2.38334	0.472146
42	326738.8836				4633.351212	-2.38286	0.47678
43	317753.3625				4631.493969	-2.38238	0.481082
44	309177.2897				4629.622178	-2.3819	0.485044
45	300989.7657				4627.737195	-2.38141	0.488659
46	293171.0651				4625.840397	-2.38092	0.491922
47	285702.5658				4623.933179	-2.38042	0.494826
48	278566.6811				4622.016949	-2.37992	0.497368
49	271746.7976				4620.093124	-2.37942	0.499545
50	265227.2163				4618.163124	-2.37892	0.501355
51	258993.0978				4616.228372	-2.37842	0.502799
52	253030.4115				4614.290285	-2.37792	0.503875
53	247325.8871				4612.350274	-2.37741	0.504585
54	241866.9699				4610.409736	-2.37691	0.504932
55	236641.7789				4608.470054	-2.3764	0.50492
56	231639.0673				4606.532592	-2.3759	0.504552
57	226848.1856				4604.598691	-2.37539	0.503834
58	222259.0472				4602.669665	-2.37489	0.502773
59	217862.0958				4600.746801	-2.37439	0.501375
60	213648.275				4598.831351	-2.37389	0.499647
61	209609.0001				4596.924534	-2.37339	0.4976
62	205736.1308				4595.027532	-2.3729	0.495241
63	202021.9465				4593.141486	-2.3724	0.492582
64	198459.1226				4591.267497	-2.37191	0.489631
65	195040.7084				4589.40662	-2.37143	0.4864
66	191760.106				4587.559869	-2.37094	0.482901
67	188611.051				4585.728209	-2.37047	0.479144
68	185587.5944				4583.912558	-2.36999	0.475143
69	182684.0844				4582.113787	-2.36952	0.470909
70	179895.151				4580.332718	-2.36905	0.466455
71	177215.6905				4578.570123	-2.36859	0.461793
72	174640.8506				4576.826724	-2.36813	0.456936
73	172166.0174				4575.103198	-2.36768	0.451896
74	169786.8025				4573.400167	-2.36724	0.446687
75	167499.0308				4571.718209	-2.36679	0.441321
76	165298.7292				4570.057852	-2.36636	0.435811
77	163182.1159				4568.419576	-2.36593	0.430168
78	161145.5907				4566.803815	-2.3655	0.424405
79	159185.7247				4565.210957	-2.36509	0.418534
80	157299.2523				4563.641346	-2.36467	0.412567
81	155483.0619				4562.095282	-2.36427	0.406514
82	153734.1884				4560.573023	-2.36387	0.400388
83	152049.8056				4559.074785	-2.36347	0.394198
84	150427.219				4557.600748	-2.36308	0.387955

85	148863.8591				4556.151049	-2.3627	0.38167
86	147357.2749				4554.725793	-2.36233	0.375351

While the result is not perfect but it is as close as it can get, without a significantly more complicated circuit.

Doing the simulation with a temperature sweep, we can see that the simulation agrees with the calculations.

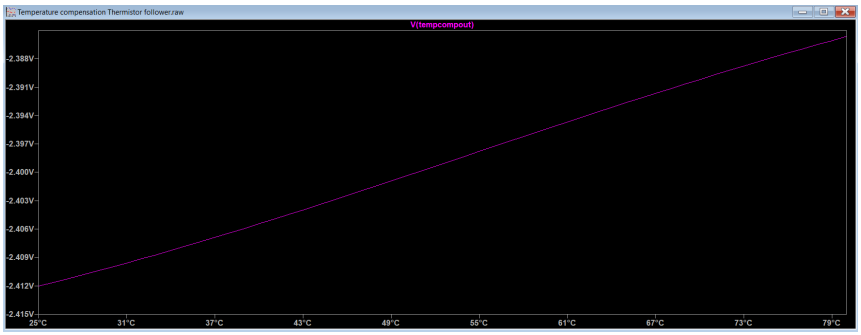


Figure 46 Output voltage vs temperature chart

5.11.1 Complete Negative Voltage switching

At this point all switching voltage circuit can be put together.

The resulting schematic is the following:

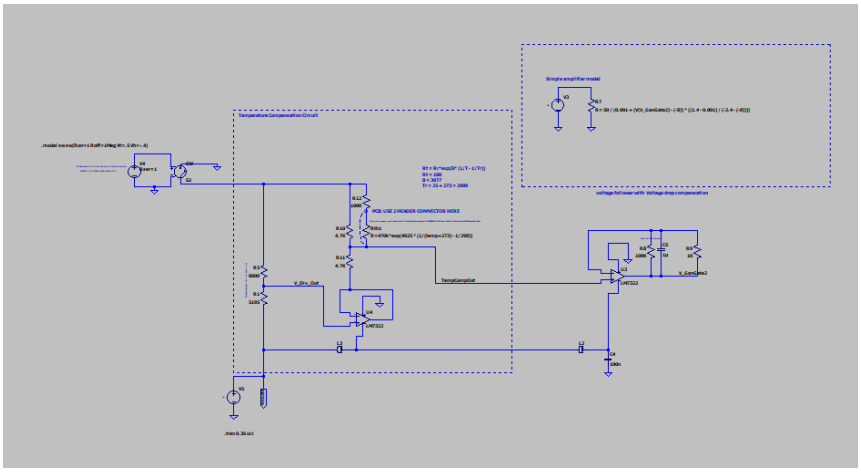


Figure 47: Complete Negative Voltage switching Schematic

After the simulation the behavior of the system is as expected

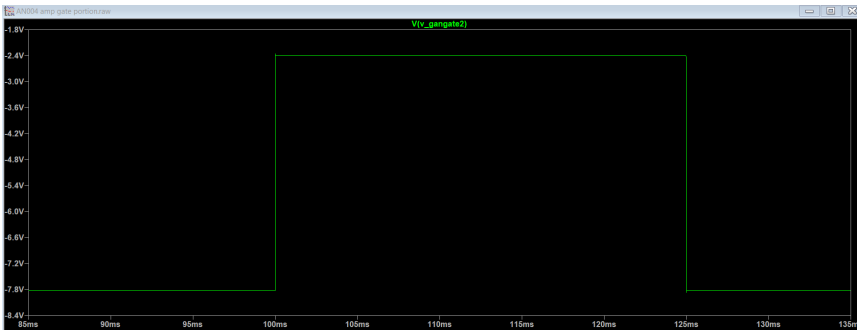


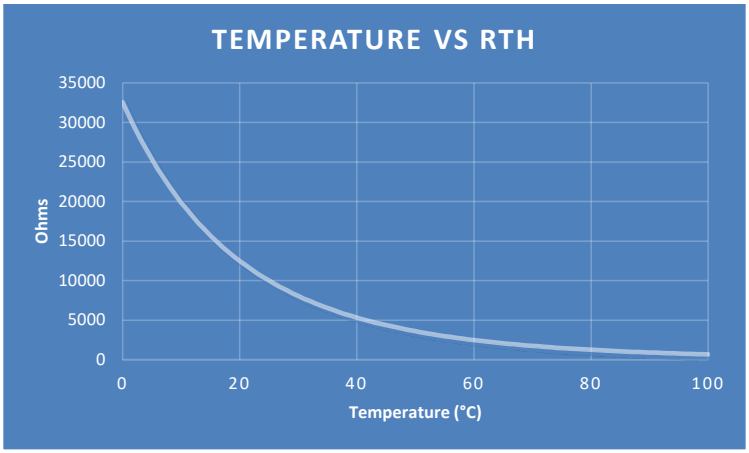
Figure 48: Verification of the negative voltage switching

5.12 Temperature Calculation and Temperature Monitoring.

5.12.1 Designing the temperature monitoring circuit.

To monitor the temperature of the amplifier another NTC (Negative temperature coefficient) thermistor must be used. The only design requirement is that it can have an operating temperature at least as high as the highest temperature that the amplifier will reach. In the end a generic 10K thermistor was selected, and more specifically the NTCLE201E3103SBA from Vishay.

The problem with the thermistors in general is that their temperature to resistance relation is highly non linear



As a result, it is fairly difficult to map the output voltage to a specific temperature. To avoid this issue, a conversion circuit was designed.

This temperature sensing circuit uses a resistor in series with a (NTC) thermistor to form a voltage divider, which has the effect of producing an output voltage that is linear over temperature. The circuit uses an op amp in a non-inverting configuration with inverting reference to offset and gain the signal, which helps to utilize the full ADC resolution and increase measurement accuracy.

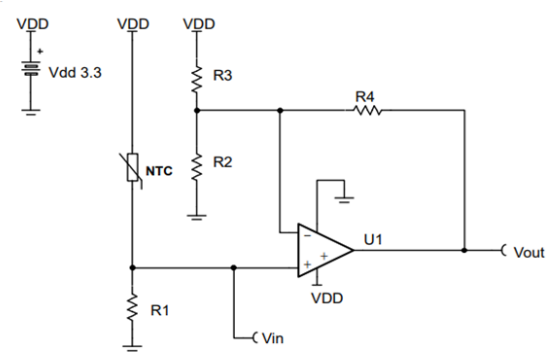


Figure 49: Circuit to convert the nonlinear behavior of a thermistor to linear voltage

Before calculating the R values, some properties must be taken into account:

- The op amp must be used in a linear operating region. Linear output swing is usually specified under the AOL test conditions. For example, for the selected op-amp the linear output swing is 0.05 V to 3.25 V.
- Low value resistors (10kΩ or less) must be used because using high value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
- A capacitor placed in parallel with the feedback resistor will limit bandwidth, improve stability and help reduce noise

The output can be found by the following equation

$$V_{out} = V_{dd} * \frac{R_1}{R_{NTC} + R_1} * \frac{(R_2 \,||\, R_3) + R_4}{(R_2 \,||\, R_3)} - \left(\frac{R_4}{R_3} * V_{dd}\right)$$

The value of R1 must be calculated to produce a linear output voltage using the minimum and the maximum of the R_{NTC} for the selected temperature range.

In the case T_{Min} = 5 °C and T_{Max} = 80 °C has been selected. The resulting resistances are:

Temperature	R_{NTC}	
5	25338	Ohmn
80	1256	Ohmn

And the R1 can now be calculated by the following equation

$$R_1 = \sqrt{R_{NTCMin} * R_{NTCMax}} = 5641\ \Omega$$

The closest standard value was 5.6KΩ so that value was selected.

The input voltage range can be calculated with the following equations:

$$V_{inMin} = V_{dd} * \frac{R_1}{R_{NTCMax} + R_1} = 0.597324V$$

$$V_{inMax} = V_{dd} * \frac{R_1}{R_{NTCMin} + R_1} = 2.695449V$$

The gain required to produce the maximum output switch of (0.05 to 3.25) can be calculated by the following equation

$$G_{ideal} = \frac{V_{outMax} - V_{outMin}}{V_{inMax} - V_{inMin}} = 1.525171\frac{V}{V}$$

We can then solve for the parallel combination of R2 || R3 using the ideal gain that was just calculated using the following equation, and with a selected R4 of 1.5KΩ

$$(R_2||R_3)_{ideal} = \frac{R_4}{G_{ideal} - 1} = 2856.2\ \Omega$$

The R2 and R3 can be calculated with the following equations based off the transfer function and the gain

$$R_3 = \frac{R_4 * V_{DD}}{V_{inMax} * G_{ideal} - V_{outMax}} = 5748.9\ \Omega$$

$$R_2 = \frac{(R_2||R_3)_{ideal} * R_3}{R_3 - (R_2||R_3)_{ideal}} = 5676.3\ \Omega$$

The closest standard resistors to that value are 5.8KΩ for both R2 and R3, so that resistors were selected. Now the actual gain can be calculated with the following equation

$$G = \frac{(R_2 | | R_3) + R_4}{(R_2 | | R_3)} = \frac{(5800 | | 5800) + 1500}{(5800 | | 5800)} = 1.5405 \frac{V}{V}$$

Using the V_out equation with the calculated resistor values and the RthMin and RthMax respectively we get

voutMin	**0.052836V**	at temperature min
VoutMax	**3.236199V**	at temperature max

= Temperature Min + (Vout – voutmin) * ((Temperature Max - Temperature Min)/(voutmax-voutmin))

Finally, from the output voltage the temperature of the thermistor can be calculated now with the following equation

$$T = T_{Min} + (V_{out} - V_{OutMin}) * \left(\frac{T_{Max} - T_{Min}}{V_{OutMax} - V_{OutMin}}\right)$$

Using an additional op-amp in a comparator configuration another simple circuit can be design that will raise an alarm when a critical voltage threshold has been reached. This be accomplished by selecting a target threshold temperature, and finding the voltage, then using a voltage divider to set that voltage as the low Input of the comparator.

The Vout can be found from the target temperature using the following equation:

$$V_{outThres} = V_{outMin} + (T_{Thres} - T_{\mathrm{Min}}) * \left(\frac{(V_{OutMax} - V_{outMin})}{T_{Max} - T_{Min}}\right)$$

And the resistor values to reach that Vout from the Vdd can be found from the standard voltage divider equation.

The final implementation to be simulated can be found on the following image.

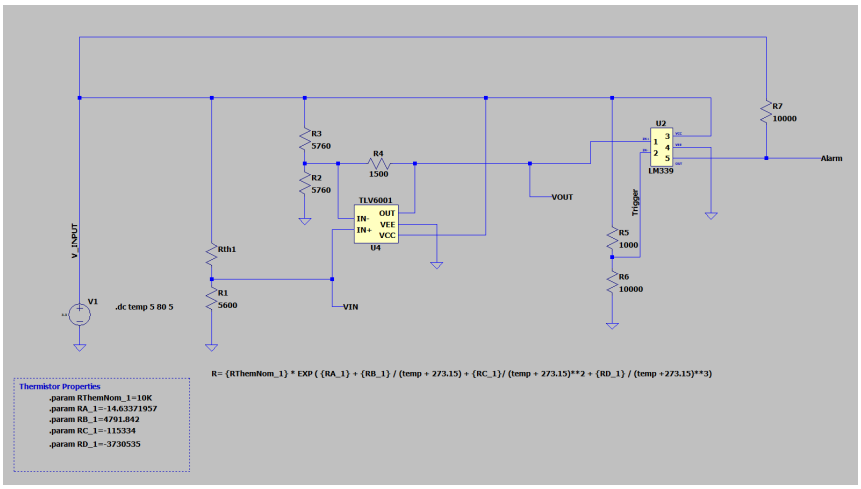


Figure 50: Proposed circuit on LtSpice for the voltage monitoring

Running the simulation using a thermal sweep we can see that the result matches the prediction of the calculations. The Vout is almost linear, and the alarm is raised on the selected threshold.

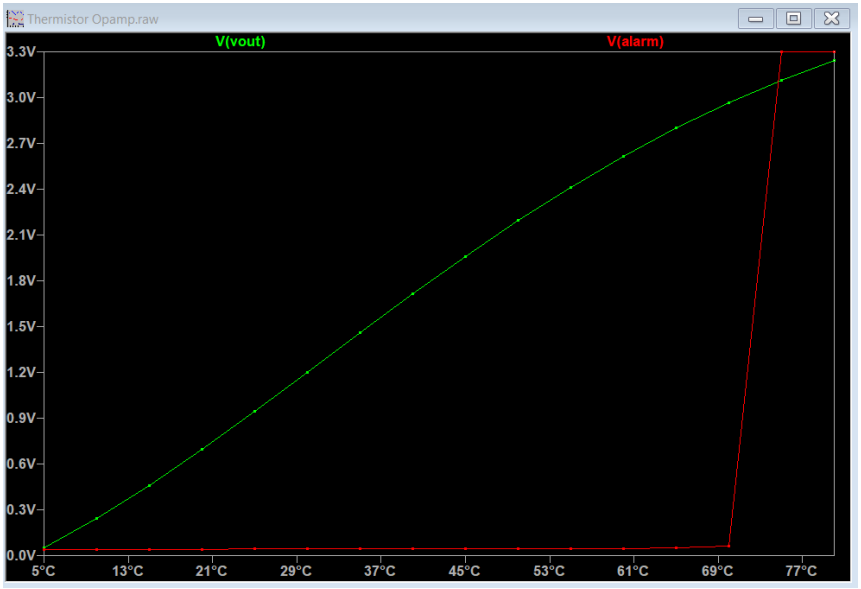


Figure 51: Simulation of the temperature Alarm

5.13 Complete system Simulation.

After putting the components of the complete system together, the resulting schematic can be seen in the following image.

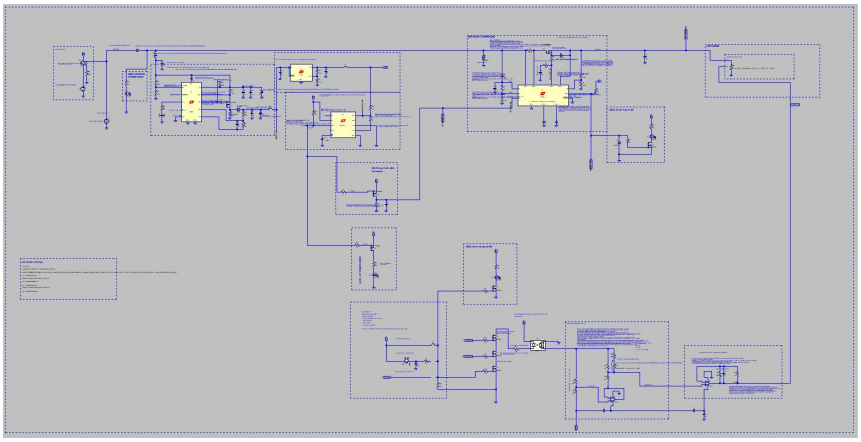


Figure 52: Complete System in LtSpice

5.14 VSWR Protection Circuit Design

Voltage Standing Wave Ratio (VSWR) is a critical parameter in RF and microwave systems, representing the efficiency of power transmission from an amplifier to a load (like an antenna). A perfect VSWR of 1:1 indicates all the power is transmitted, while higher ratios imply reflections due to impedance mismatches, leading to power being reflected back into the amplifier.

In Power Amplifiers (PAs), high VSWR levels can be detrimental, causing damage due to the reflected power. A VSWR Protection Circuit is essential to monitor these levels and ensure safe operation. It detects unacceptable VSWR conditions, often triggering protective mechanisms like reducing output power or shutting down the amplifier to prevent damage. This circuit is vital for maintaining the amplifier's longevity and reliability, especially in systems where variable or unpredictable load conditions are common. This specific power amplifier can survive a VSWR of 7 up to 100ms, so for this reason, as well as the cost of this amplifier, it is for critically importance to have an electronic protection build in, which can raise an alarm. This alarm can then be

intercepted by a microcontroller using an interrupt, which can in turn of automatically the RF source in a few ms.

The ADL5519 is a key component in the current VSWR Protection Circuit design, serving as a dual logarithmic detector. It excels in measuring RF power and converting it into a corresponding voltage level, which can then in turned, measured if needed. The ADL5519's dual-channel nature allows for simultaneous measurement of forward and reverse power levels, which are crucial for accurate VSWR calculation.

This detector operates over a wide frequency range, making it well-suited for diverse RF applications. It provides logarithmic voltage outputs that represent the RF signal power, enabling the system to calculate VSWR by comparing the forward and reflected power levels. Its high accuracy and fast response time make the ADL5519 an ideal choice for real-time VSWR monitoring, ensuring prompt detection of any impedance mismatches. By integrating the ADL5519 into the VSWR Protection Circuit, the system can reliably protect the power amplifier from the potentially damaging effects of high VSWR levels.

This is the proposed circuit from the manufacturer’s datasheet.

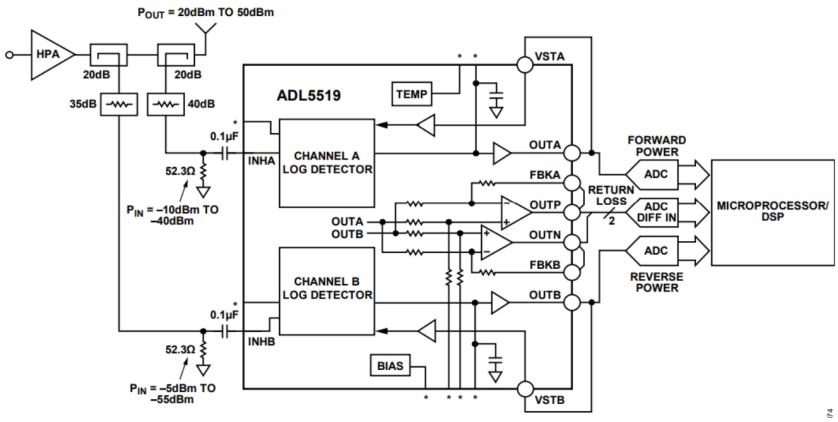


Figure 53: Vswr Application example

The OUTA and OUTB pins output a voltage depending on the power that inputs on the coupler.

The OUTA and OUTB voltage follow the following curve.

V_P = 5 V; T_A = +25°C, −40°C, +85°C; CLPA, CLPB = 1 µF. Colors: +

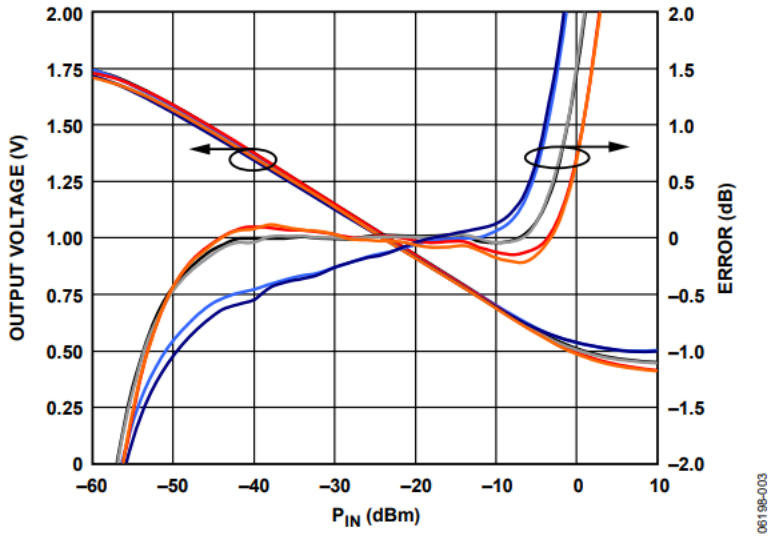


Figure 3. OUTA, OUTB Voltage and Log Conformance vs. Input Amplitude at 100 MHz, Typical Device, ADJA, ADJB = 0.65 V, 0.7 V, Sine Wave, Single-Ended Drive

Figure 54: ADL5519 Voltage vs power response

It is clear thet the effective power input that can be added on the ADL5519 is from -60dBm to -5dBm, because thats the range where the voltage output is linear.

The Adl outputs voltage values proportional to the log of the power levels at its inputs. This means that the difference between the output voltages (OUTA - OUTB) corresponds to the difference between the logs of the forward and reverse power levels in dB.

To calculate the power level (in dBm) for a given output voltage (x) between 1.75V and 0.6V, we can use linear interpolation. Linear interpolation assumes that the relationship between voltage and power is linear (which in this case it is), and uses this assumption to estimate the power level at the desired voltage based on the known power levels at two nearby voltages.

$$y = y_0 + (x - x_0) * \frac{(y_1 - y_0)}{x_1 - x_0}$$

More specifically

$$Power_{dBm} = Power_{min} + (voltage - voltage_{atMinPower}) * \frac{power_{max} - power_{min}}{Voltage_{atMinPower} - Voltage_{atMaxPower}}$$

Since (OUTA - OUTB) corresponds to the difference between the logs of the forward and reverse power levels in dB, we can calculate the return loss as

$$ReturnLoss_{dB} = ForwardPower_{dBm} - ReversePower_{dBm}$$

From that, we can find the reflection coeeficient Γ using

$$\Gamma = 10^{-\left(\frac{ReturnLoss_{dB}}{20}\right)}$$

Then finally the vswr can be calculated as:

$$VSWR = \frac{1 + \Gamma}{1 - \Gamma}$$

To give an example with numbers we have

OUTA = 0.6V -> Forward Power = -5dBm

OUTB = 1.6V -> Reverse Power = -52.8dBm

Return loss (dB) = 47.8

Reflection Coefficient Γ = 0.004

VSWR = 1.008

5.14.1 Differential output.

Besides OUTA and OUTB it also has the differential outputs.

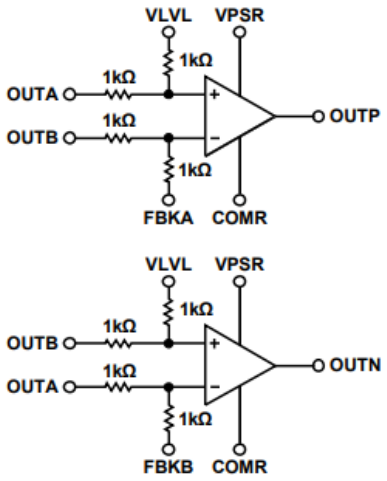


Figure 55: OUTP and OUTN pins of ADL5519

If OUTP is connected to FBKA, OUTP is given as

$$OUTP = OUTA - OUTB + VLVL$$

If OUTN is connected to FBKB, OUTN is given as

$$OUTN = OUTB - OUTA + VLVL$$

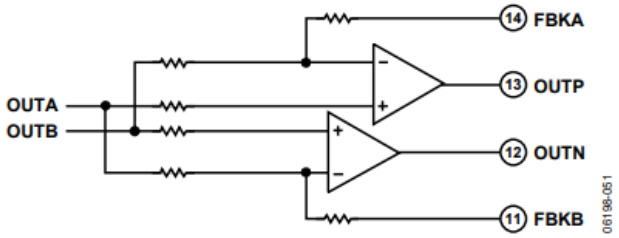


Figure 56. Relationship between the OUTA and OUTB pins, and differential outputs

A differential output can be taken from OUTP − OUTN, and VLVL can be used to adjust the common-mode level for an ADC connection. This is convenient not only for driving a differential ADC but also for removing any temperature variation on VLVL

$$OUTP = (OUTA - OUTB + VLVL)$$

$$OUTN = (OUTB - OUTA + VLVL)$$

The problem is that without offset (and with the example numbers that i demonstrated above) at points the OUTP will be negative. To counter this we can use a minimum of 1.15V voltage in the VLVL pin of the IC to offset the whole differential system by that amount. In the end a 2V offset was selected for convenience because we can add directly voltage reference with that output. . With 2V offset the at worst case scenario the OUTP will be 1V

5.14.2 Using the OUTP and OUTN for alarm generation when the vswr is exceeded

As a first step, the OUTP and OUTN interface was recreated in Ltspice, to behave as described on the datasheet.

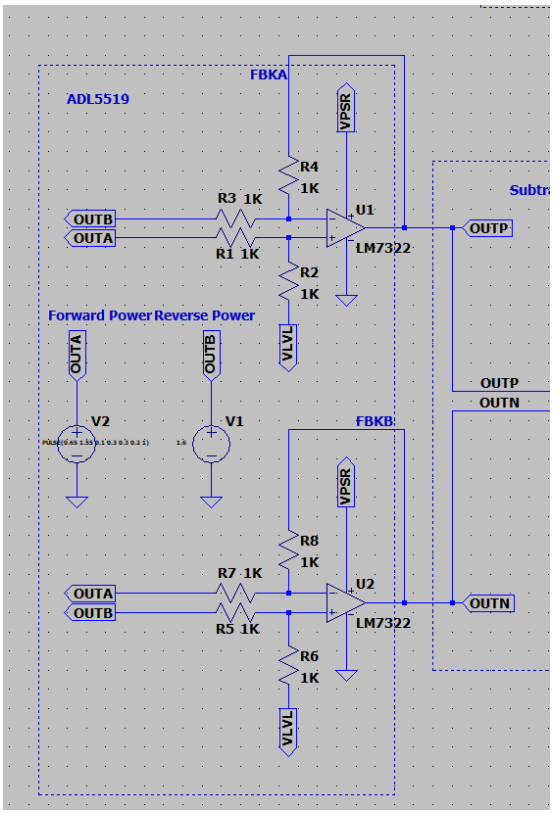


Figure 57: Differential output simulated in LtSpice

Then a sweep was added on the OUTA, starting from 0.64V to 1.55V

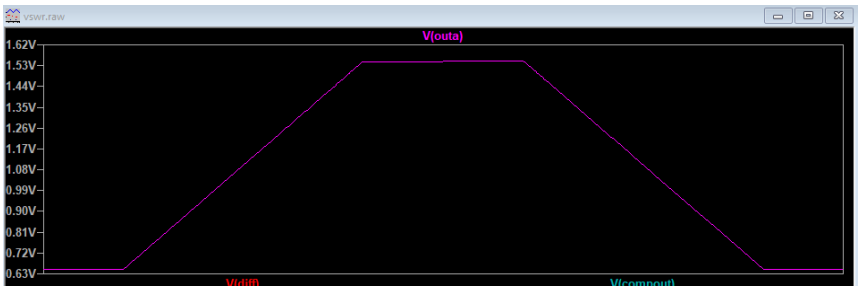


Figure 58: OutA Voltage Sweep input parameter

To verify that, yes, the OUTP and OUTN outputs the voltage that it is expected (and it follows the equation of the datasheets)

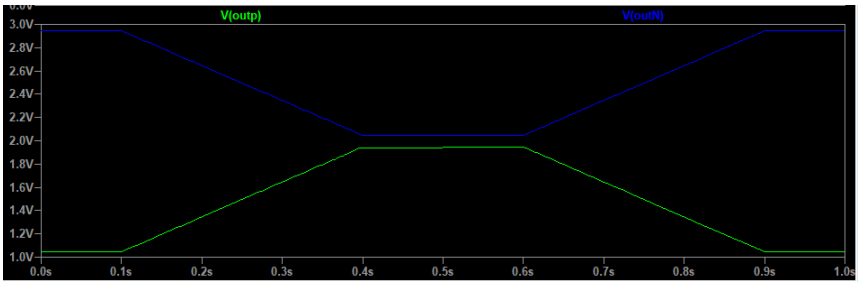


Figure 59: Differential Output on voltage Sweep of OutA

After this point, another OpAmp was added in a subtractor configuration, so that it automatically outputs the voltage output between OUTP and OUTN

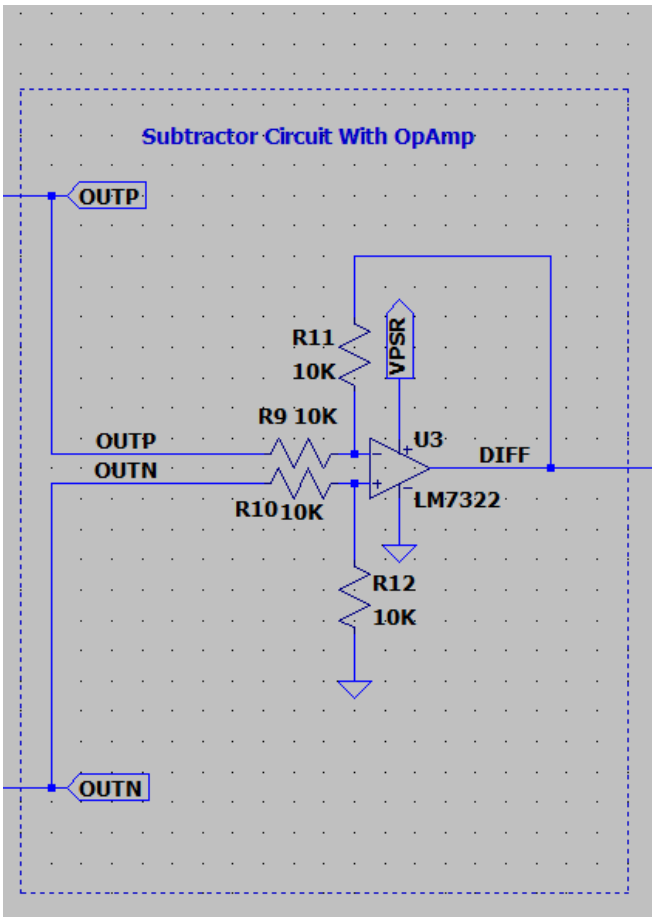


Figure 60. Circuit that subtracts 2 voltages

We know from the manufacturer that the amplifier can survive a maximum vswr of 7:1.

	Out A (FP)	0.6	-5	(
9.45	OUT B (RP)	0.7	-9.782608696	(
	Difference (or return loss) (Forward Vs Reverse) (db)	-0.1	4.782608696	
	Reflection coefficient (Γ)	0.576593265		
	Calculate the VSWR (1 + Γ) / (1 - Γ)	3.723590426		
	Lets do the same using the OUTP And N			
		Voltage	dBm	
	Out A	0.6	-5	
	Out B	0.7	-9.782608696	
	Then we have the following equations			
	OUTP = (OUTA - OUTB + VLVL)	1.9		P must g
	OUTN (OUT B - OUT A + VLVL)	2.1		
	putting this on the ADC we have	-0.2		
	put this on the ADC inverted	0.2	<0.2 limit (3.7 vswr)	

Playing with the values of the forward power and reverse power in an excel excel, we can see that the amplifier is safe when the v_Diff is more than 0.2V

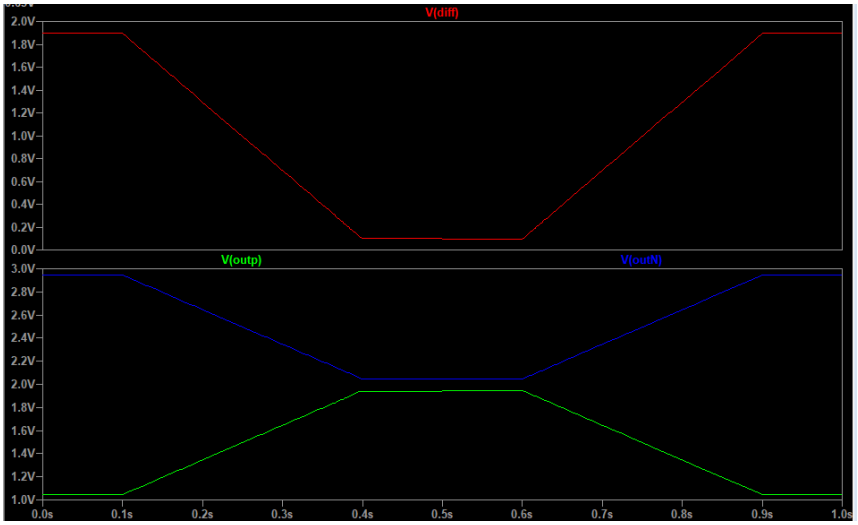


Figure 61. Subtraction of Outp and OutN.

So after the Diff/Subtracted voltage, a comparator OpAmp with open drain output was added.

Diff gets on the **In-** input. When diff is > 0.2V output will be Active **LOW**. The oOtput will be HIGH-Z, ie 3.3V because of the R13, and R16 voltage divider network and the R17 pullup resistor.

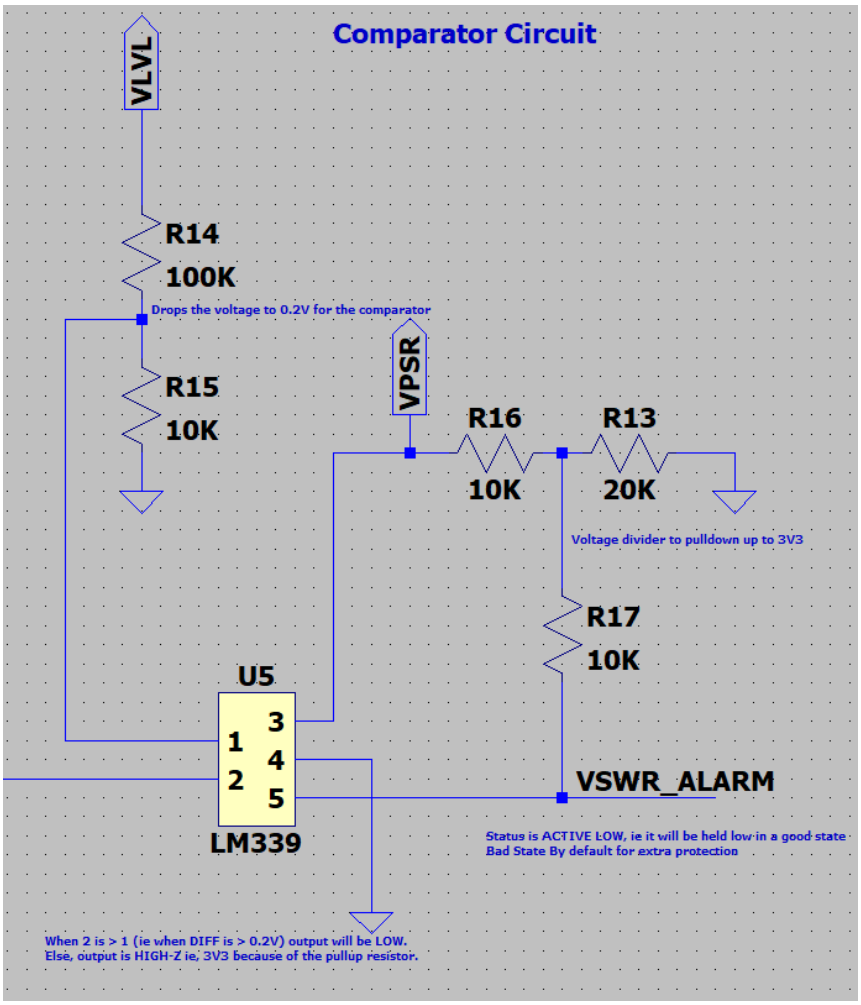


Figure 62. The OpAmp That generates the vswr alarm

And the final schematic

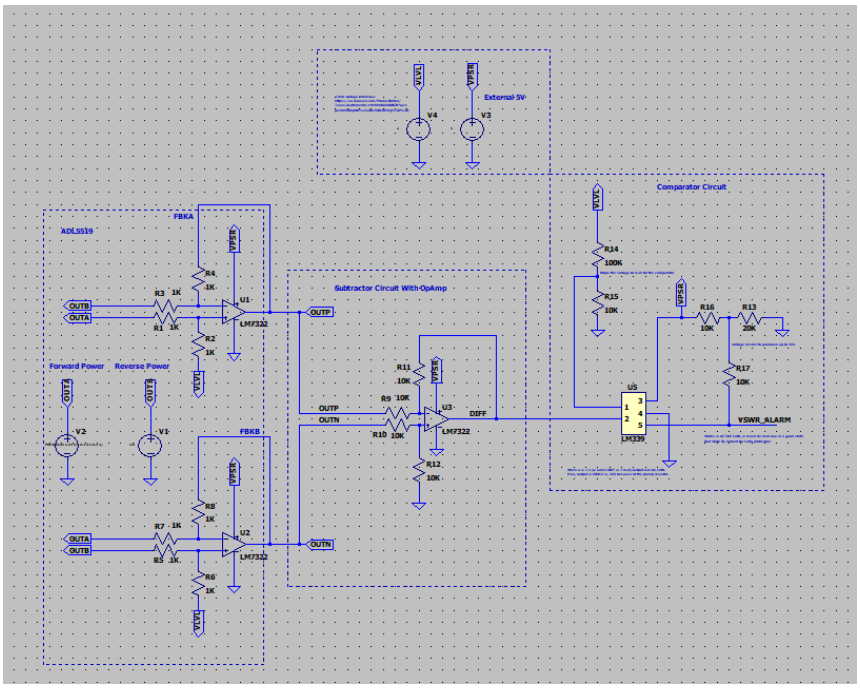
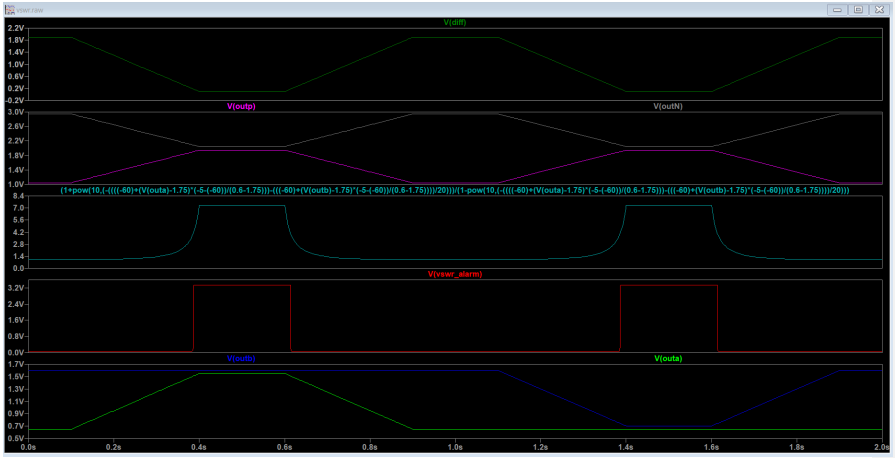


Figure 63: Final schematic of the vswr simulation

When the system was simulated again to verify that the behavior is as expected.



The actual vswr was plotted in ltspice using this beautiful equation

$$\frac{1 + pow\left(10, \left(-\frac{\left(\left((-60) + (V(outa) - 1.75) * \frac{-5-(-60)}{0.6-1.75}\right)\right) - \left(\left((-60) + (V(outb) - 1.75) * \frac{-5-(-60)}{0.6-1.75}\right)\right)}{20}\right)\right)}{1 - pow\left(10, \left(-\frac{\left(\left((-60) + (V(outa) - 1.75) * \frac{-5-(-60)}{0.6-1.75}\right)\right) - \left(\left((-60) + (V(outb) - 1.75) * \frac{-5-(-60)}{0.6-1.75}\right)\right)}{20}\right)\right)}$$

6 PCB design.

This chapter, is about the process of designing a Printed Circuit Board (PCB) for the Gallium Nitride amplifier system controller.

A printed circuit board is a rigid structure that contains electrical circuitry made up of embedded metal surfaces called traces and larger areas of metal called planes. Components are soldered to the board onto metal pads, which are connected to the board circuitry. This allows components to be interconnected. A board can be composed of one, two, or multiple layers of circuitry.

Circuit boards are built with a dielectric core material with poor electrical conducting properties to ensure pure circuitry transmission and interspaced with extra layers of metal and dielectric as needed. The standard dielectric material used for circuit boards is a flame-resistant composite of woven fiberglass cloth and epoxy resin, known as FR-4, while the metal traces and planes for the circuitry are usually composed of copper.

The PCB is not merely a platform for mounting components; it is a critical element that bridges the theoretical design with practical application. This chapter will walk through the systematic approach adopted in creating a PCB that meets the specific requirements of our GaN amplifier.

6.1 PCB design

Before a printed circuit board can be built, it must be designed. This is accomplished using PCB circuit board design CAD tools. PCB design is broken into two main categories: schematic capture to create the circuitry connectivity in a diagram and then PCB layout to design the actual physical circuit board.

The first step is to develop the library CAD parts needed for the design. This will include schematic symbols, simulation models, footprints for PCB layout

Once the libraries are ready, the next step is to create the logical representation of the circuitry on a schematic

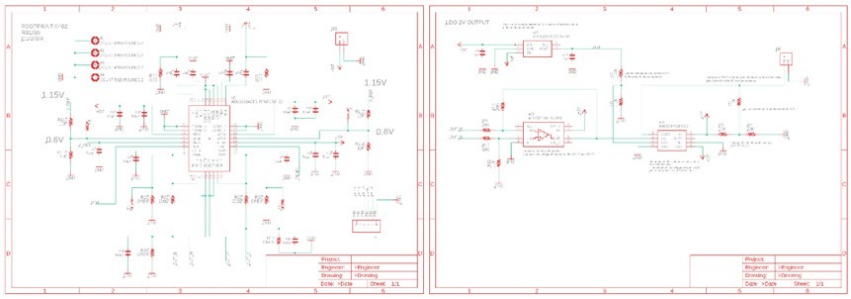


Figure 64 Schematic of the VSWR protection board.

On the layout side of PCB design, the schematic connectivity is received and processed as nets that connect two or more component pins. With an outline of the intended board shape on the screen, the component footprints are placed in the correct locations. Once these components are optimally organized, the next step is to connect the nets to the pins by drawing the traces and planes between the pins. The CAD tools have design rules built into them that prevent the traces of one net from touching another net as well as governing many other widths and spaces needed for a complete design. Once the routing is complete, the design tools are used again to create manufacturing drawings and the output files that the manufacturer will use to build the board.

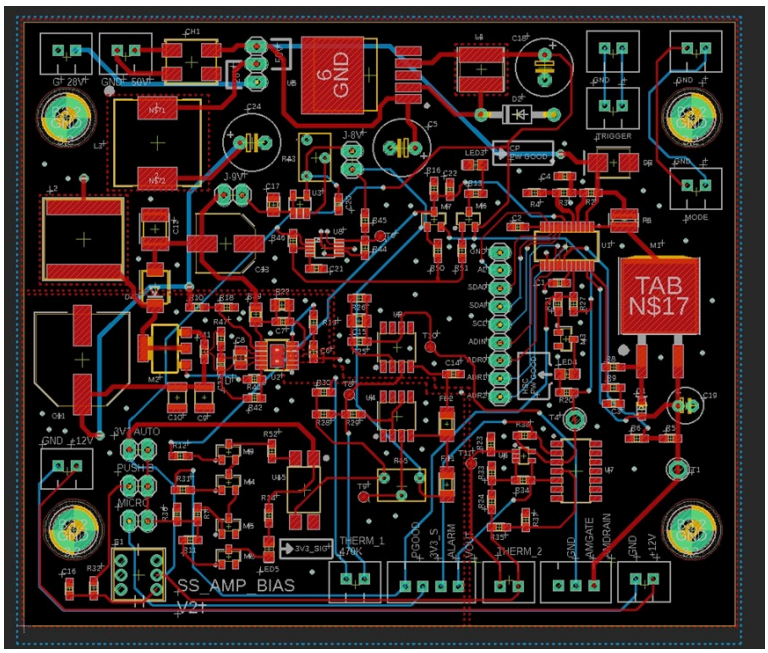


Figure 65: Board view of the V2 Bias Controller board

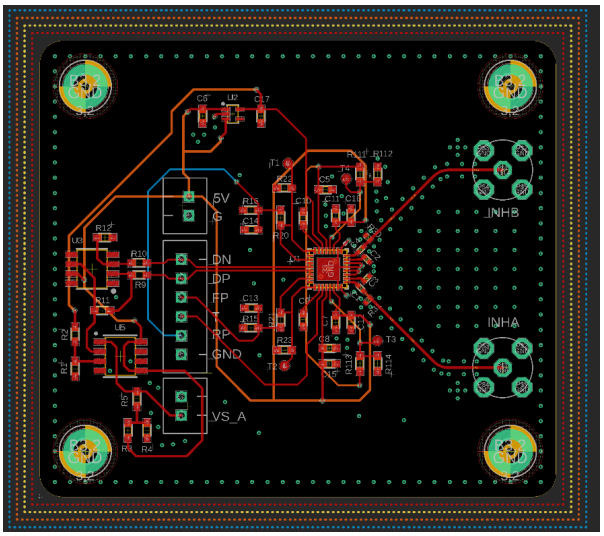


Figure 66: Board View of the VSWR protection pcb

At this point, the board is ready to be built, and the first step is to send the output data files to a facility for fabrication. This process includes etching all of the traces and planes onto the different metal layers and compressing them together, producing a bare board that is ready for assembly.

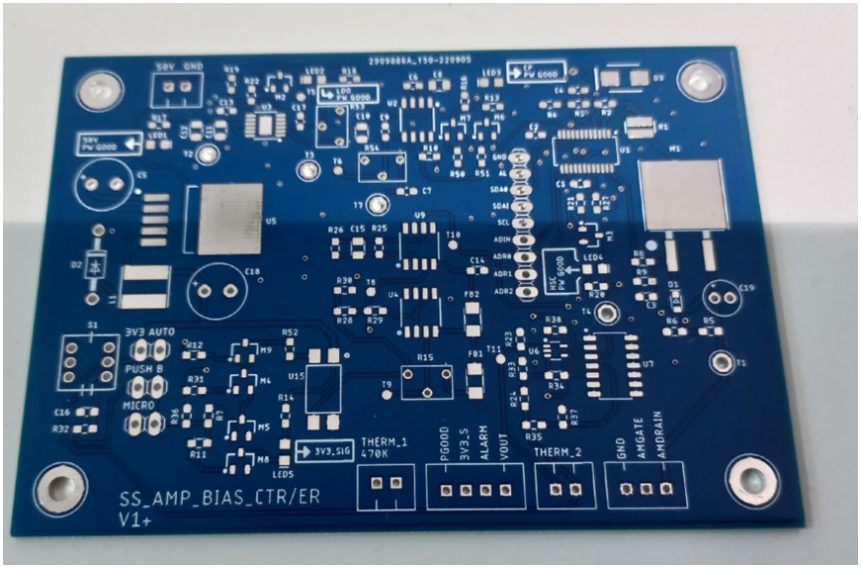


Figure 67. Blank Bias Controller Pcb

The PCB was assembled and tested, but it had some noise problems. The switching frequency of the power supply would propagate to negative noise generation.

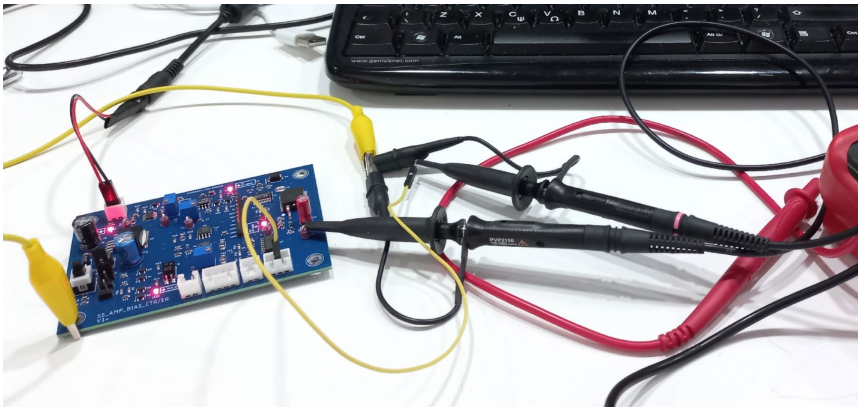


Figure 68: Testing of the Bias Controller

Figure 69: Noice issue in the negative line (blue color)

As a result, another revision was produced which had additional input filtering.

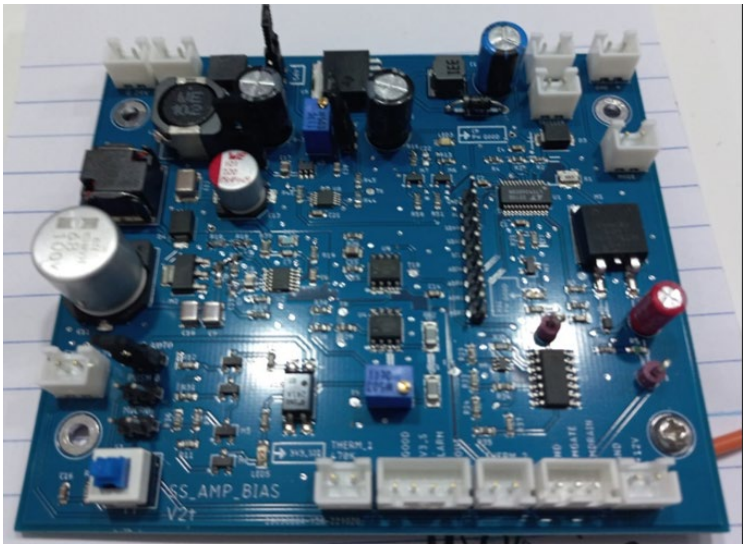
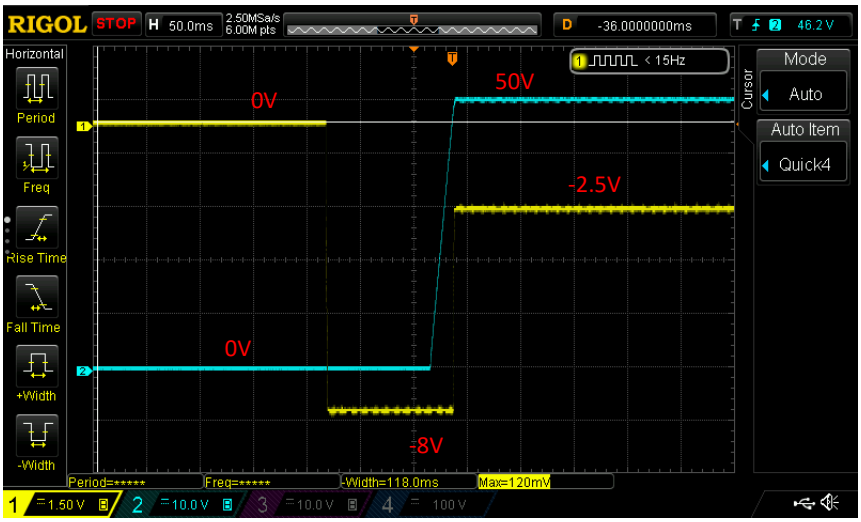


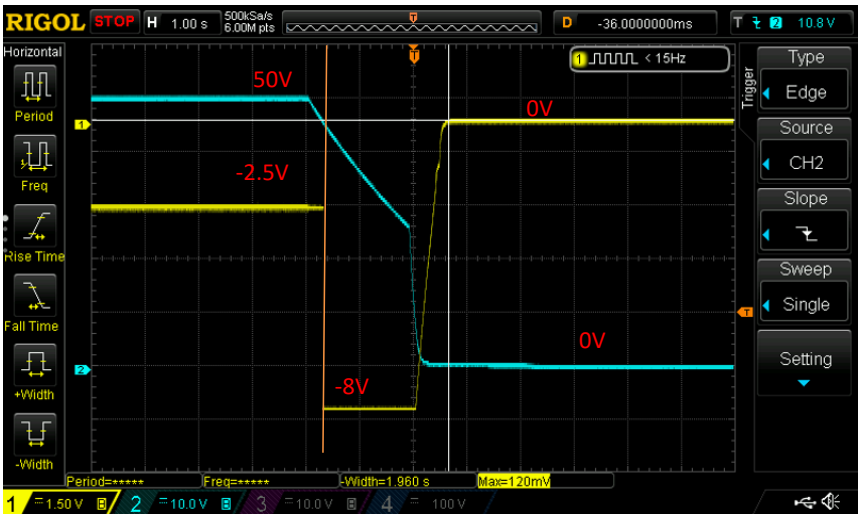
Figure 70: Assembled PCB V2 of the bias controller.

The new pcb was powered up and thoughtly tested to ensure that the actual circuit behaves like the simulations.

It does. In the following image which was taken from an osciloscope we can see the behavior of the Drain (blue line), in relation to the Gate voltage (yellow line), and that the automatic activation is started at 28V as we have calculated.



Similarly we can see that on power off, the sequencing is still behaving as expected, with the gate automatically deactivating on the correct voltages.



Similarly the VSWR protection was tested and its behaving as expected.

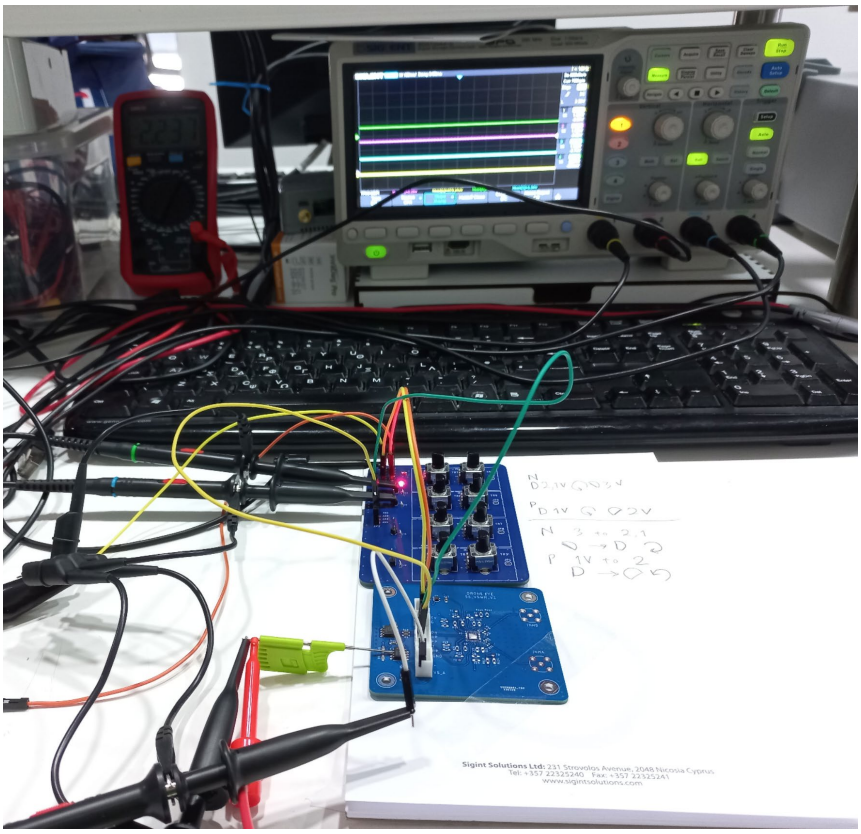


Figure 71. Testing of the alarm portion of the vswr circuit

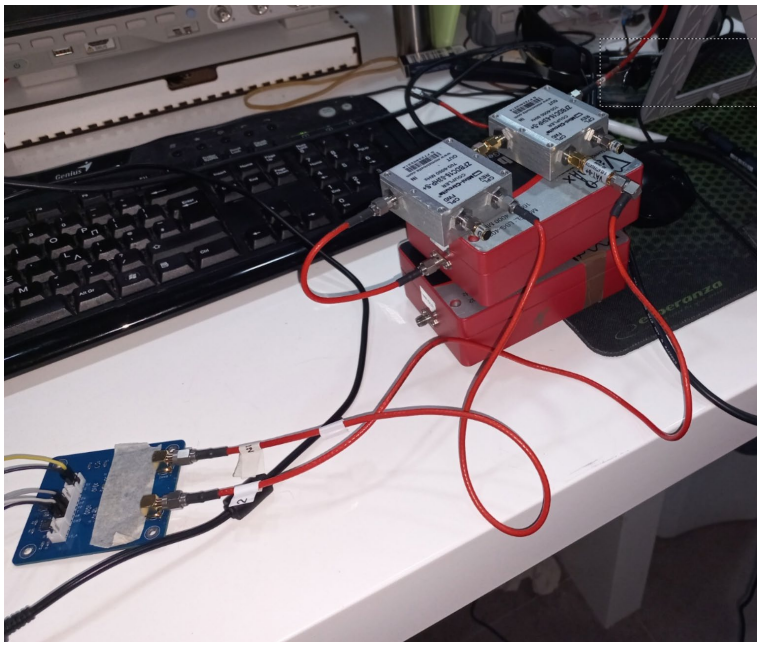


Figure 72. Testing of the complete circuit using low Power RF signals

7 Outro.

In concluding this thesis, we went through a comprehensive examination of jamming in cybersecurity and the intricate technology of Gallium Nitride (GaN) amplifiers, culminating in the practical realization of a PCB design. This work not only contributes to the academic discourse in these fields but also bridges the gap between theoretical knowledge and its practical application in advanced electronics. It is hoped that the findings and methodologies presented herein will aid in furthering research and development in the rapidly evolving domains of communication and electronic defence systems, offering a foundation for future technical advancements.

8 Table Of Figures

9 Bibliography

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